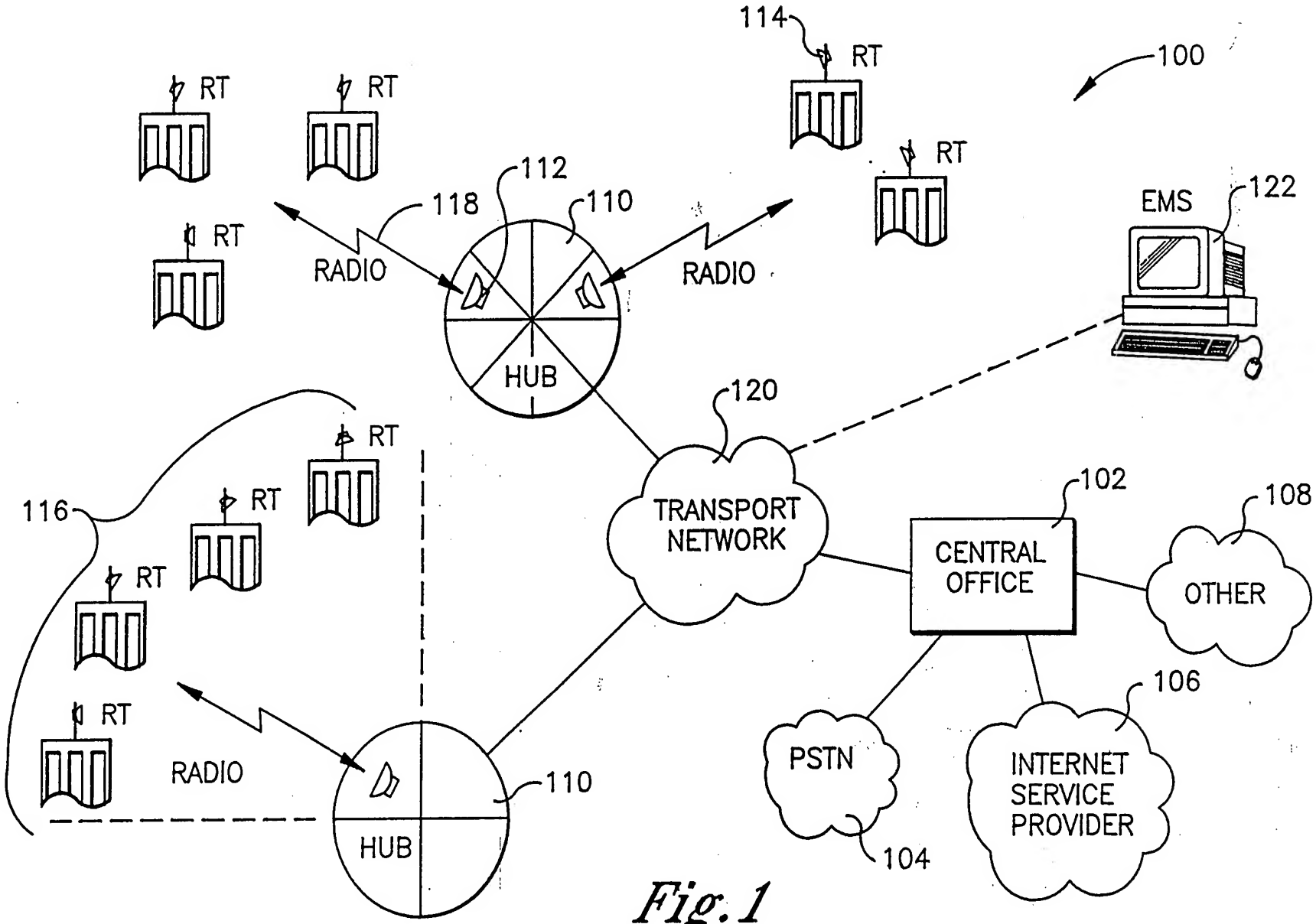

114
RT
100
RT
RT
RT
RT
112
118
110
RADIO
RADIO
EMS
122
HUB
120
RT
RT
116
RT
TRANSPORT NETWORK
102
108
CENTRAL OFFICE
OTHER
RT
RT
106
PSTN
INTERNET SERVICE PROVIDER
RADIO
110
HUB
104

Fig. 1

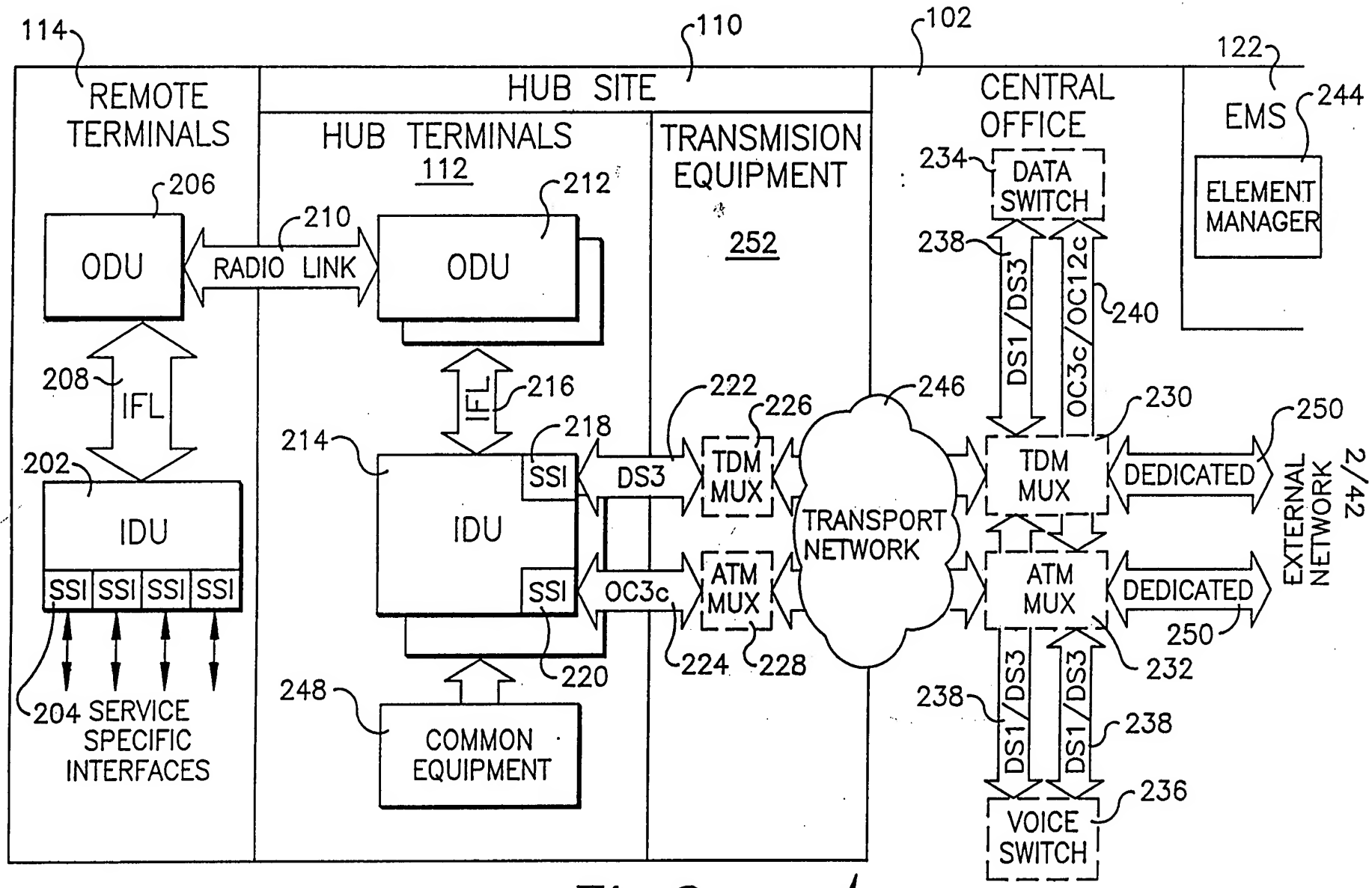

114
REMOTE TERMINALS
110
HUB SITE
102
CENTRAL OFFICE
122
EMS
244
HUB TERMINALS
112
TRANSMISION EQUIPMENT
252
206
ODU
210
RADIO LINK
212
ODU
234
DATA SWITCH
ELEMENT MANAGER
238
DS1/DS3
OC3c/OC12c
240
208
IFL
216
IFL
222
226
246
230
250
218
214
SSI
DS3
TDM MUX
TRANSPORT NETWORK
TDM MUX
DEDICATED
EXTERNAL NETWORK
202
IDU
IDU
SSI
SSI
SSI
SSI
SSI
OC3c
ATM MUX
ATM MUX
DEDICATED
250
220
224
228
232
238
DS1/DS3
DS1/DS3
238
204 SERVICE SPECIFIC INTERFACES
248
COMMON EQUIPMENT
236
VOICE SWITCH
2/42

Fig. 2

200

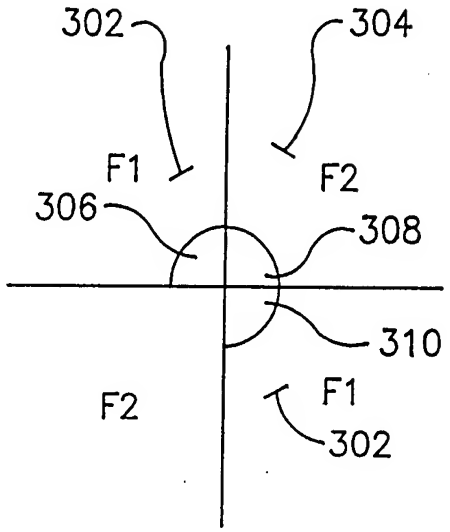


Fig. 3A

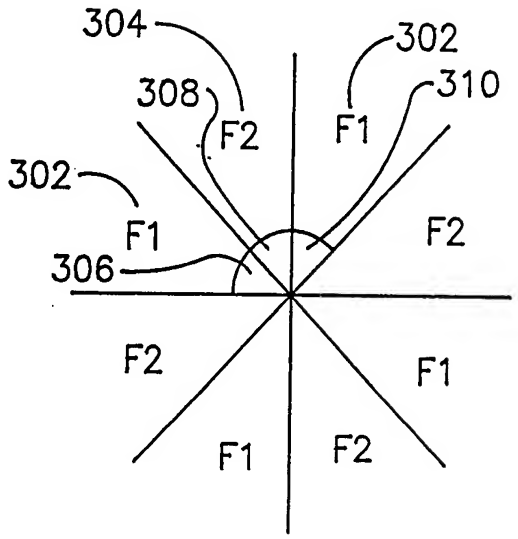


Fig. 3B

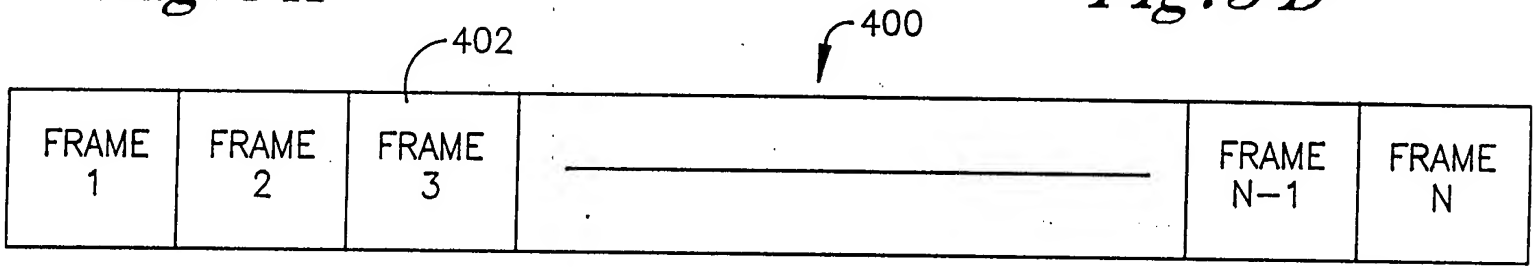


Fig. 4

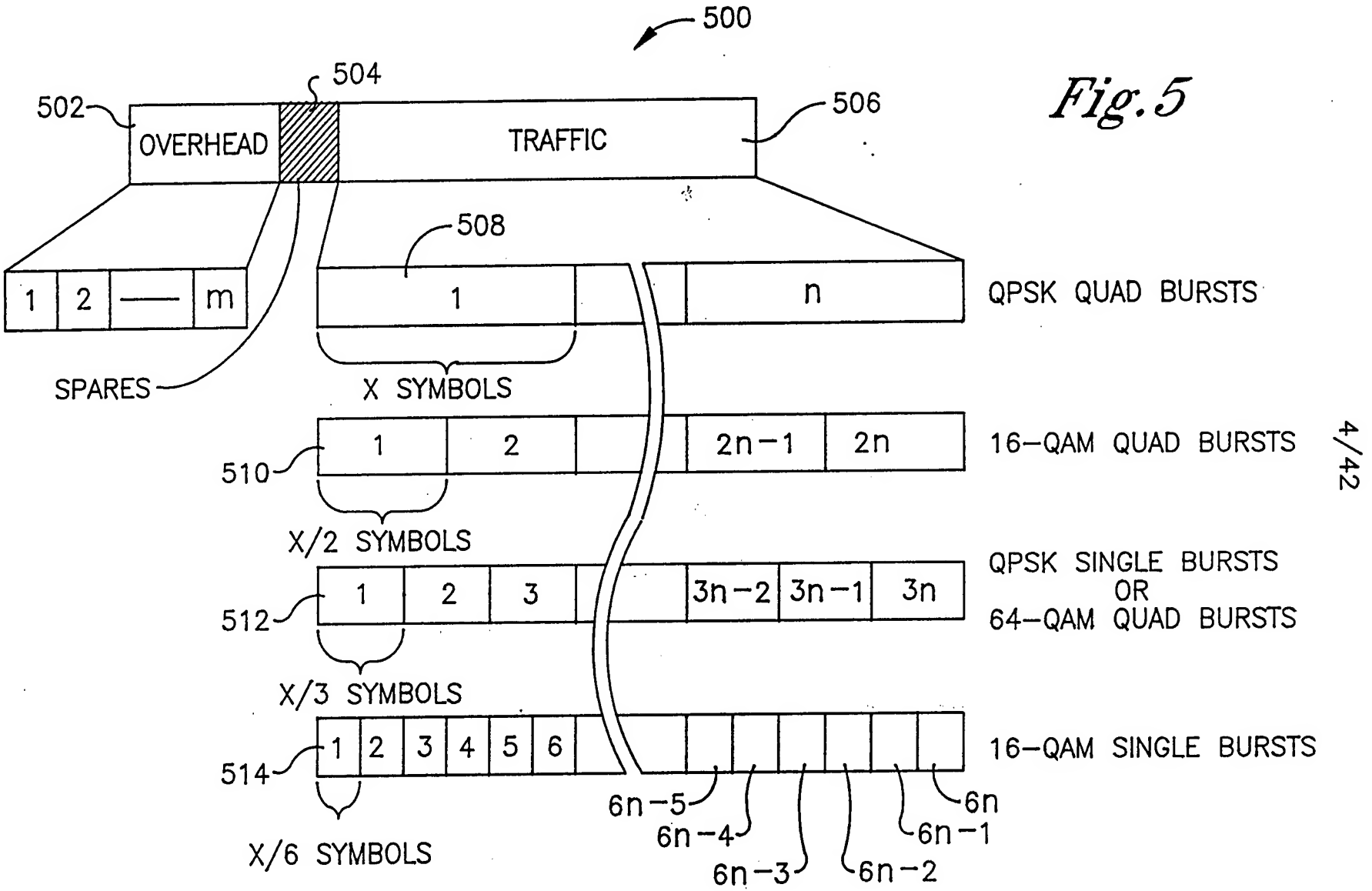

500
502
504
506
OVERHEAD
TRAFFIC
1
2
m
SPARES
508
1
n
X SYMBOLS
QPSK QUAD BURSTS
510
1
2
2n−1
2n
X/2 SYMBOLS
16−QAM QUAD BURSTS
512
1
2
3
3n−2
3n−1
3n
X/3 SYMBOLS
QPSK SINGLE BURSTS
OR
64−QAM QUAD BURSTS
514
1
2
3
4
5
6
X/6 SYMBOLS
16−QAM SINGLE BURSTS
6n−5
6n−4
6n−3
6n−2
6n−1
6n

Fig. 5

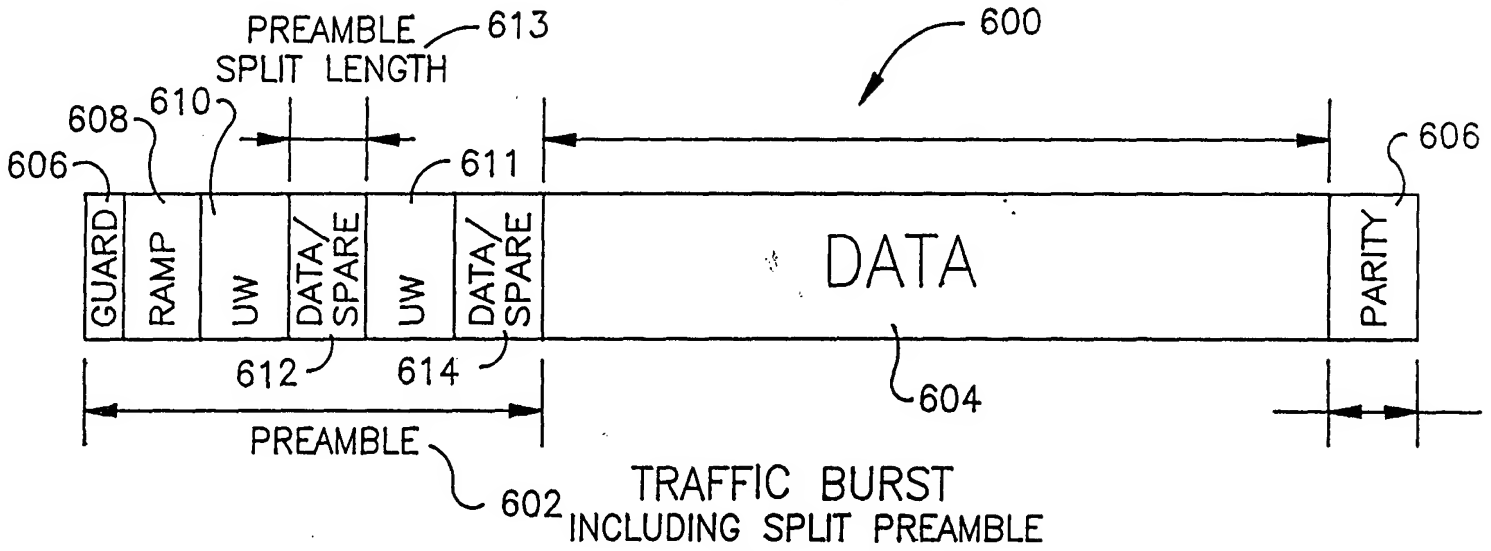


Fig. 6

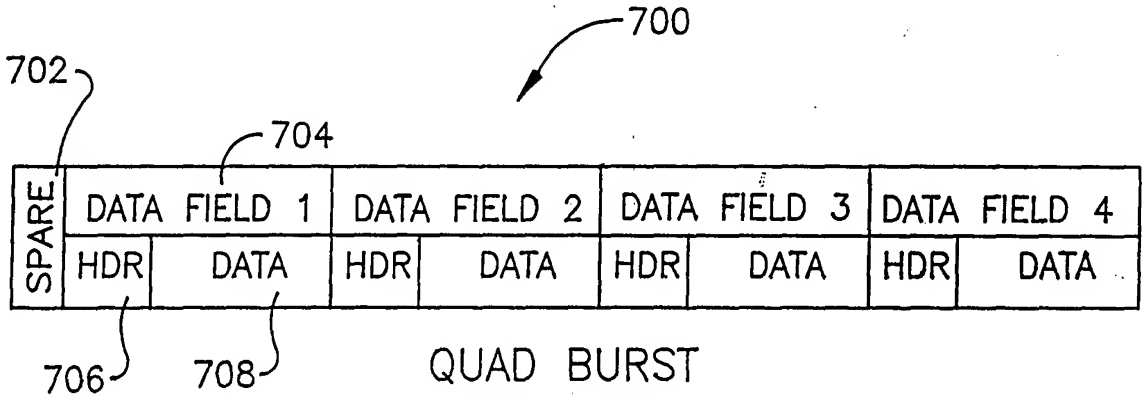


Fig. 7A

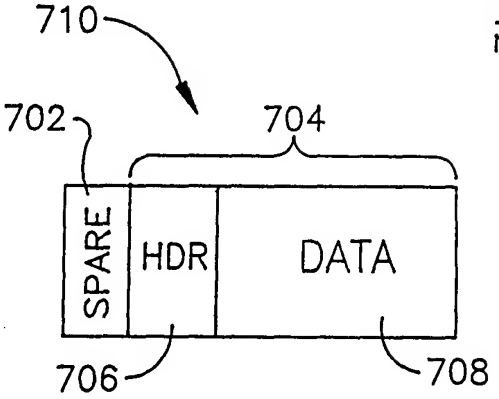


Fig. 7B

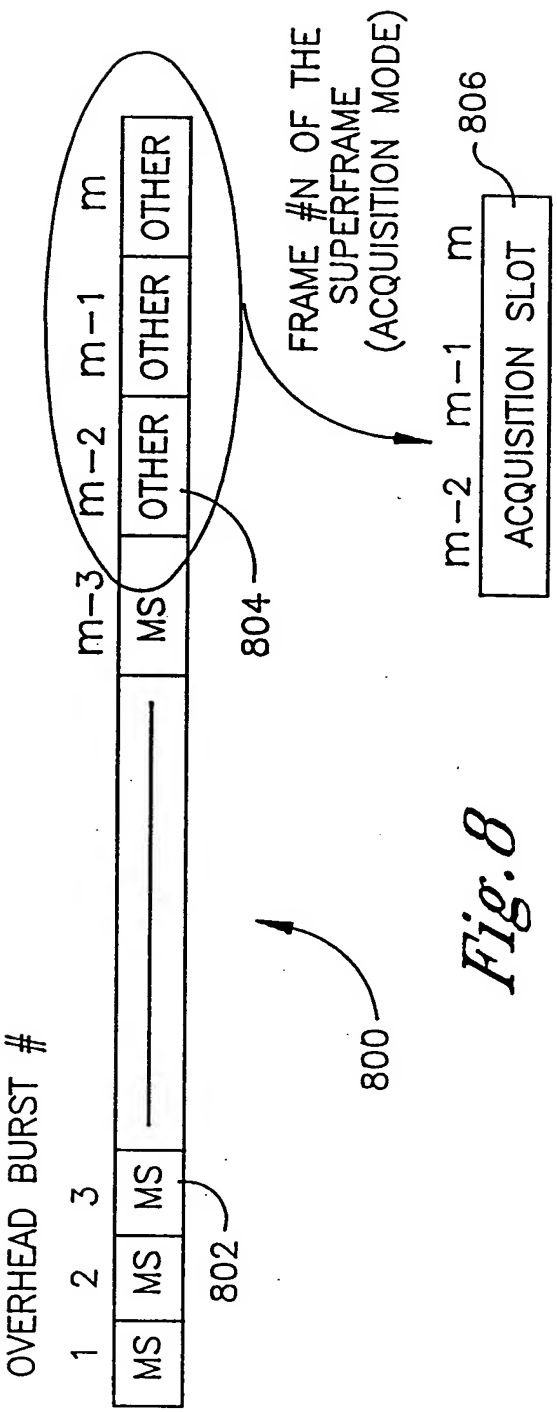

OVERHEAD BURST #
1 2 3
MS MS MS
802
800
m-3 m-2 m-1 m
MS OTHER OTHER OTHER
804
FRAME #N OF THE SUPERFRAME (ACQUISITION MODE)
m-2 m-1 m
ACQUISITION SLOT
806

Fig. 8

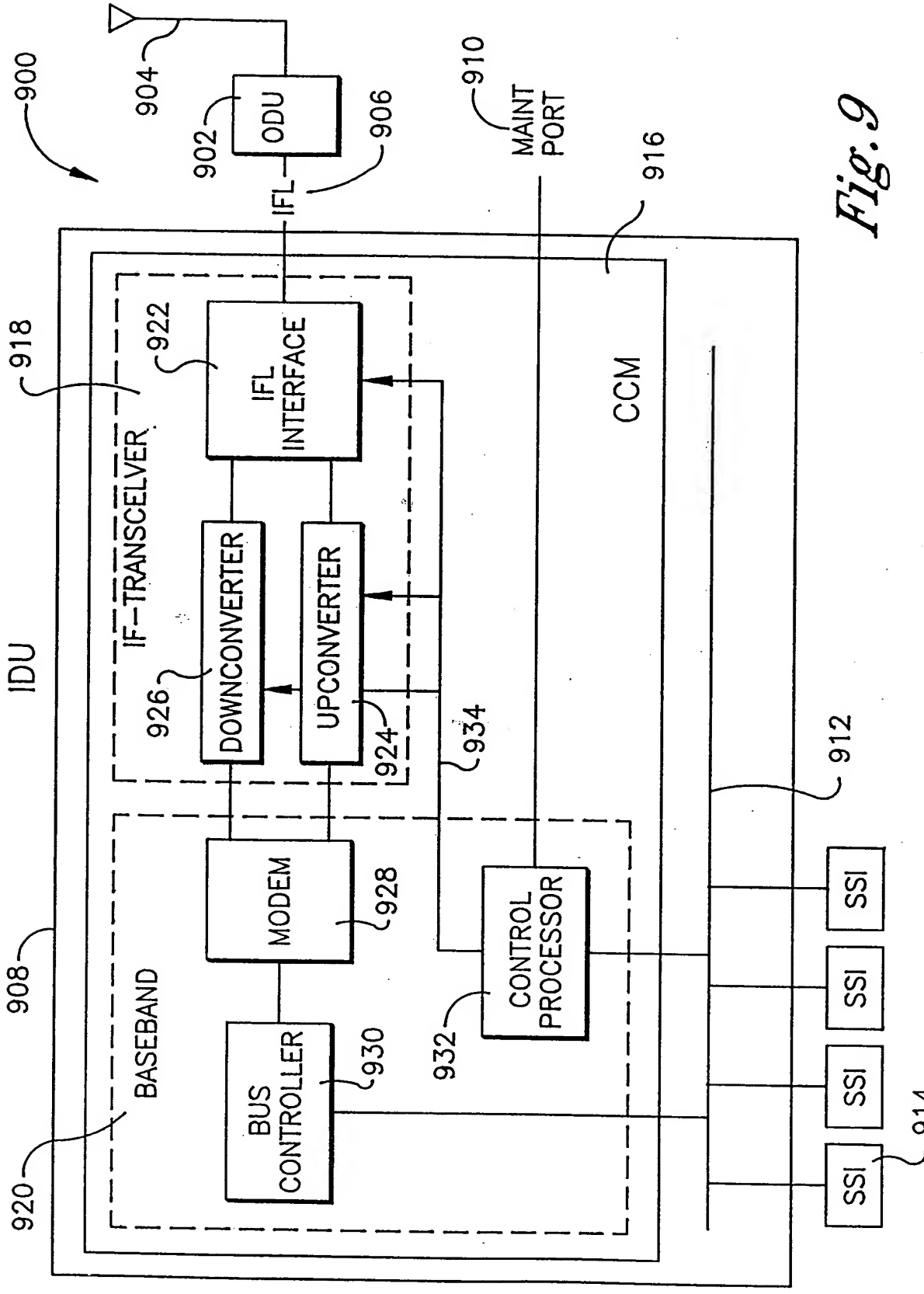

900
904
902
ODU
906
IFL
910
MAINT PORT
916
IDU
918
IF-TRANSCELVER
922
IFL INTERFACE
CCM
926
DOWNCONVERTER
UPCONVERTER
924
934
912
908
BASEBAND
MODEM
928
CONTROL PROCESSOR
SSI
SSI
SSI
SSI
914
920
BUS CONTROLLER
930
932

Fig. 9

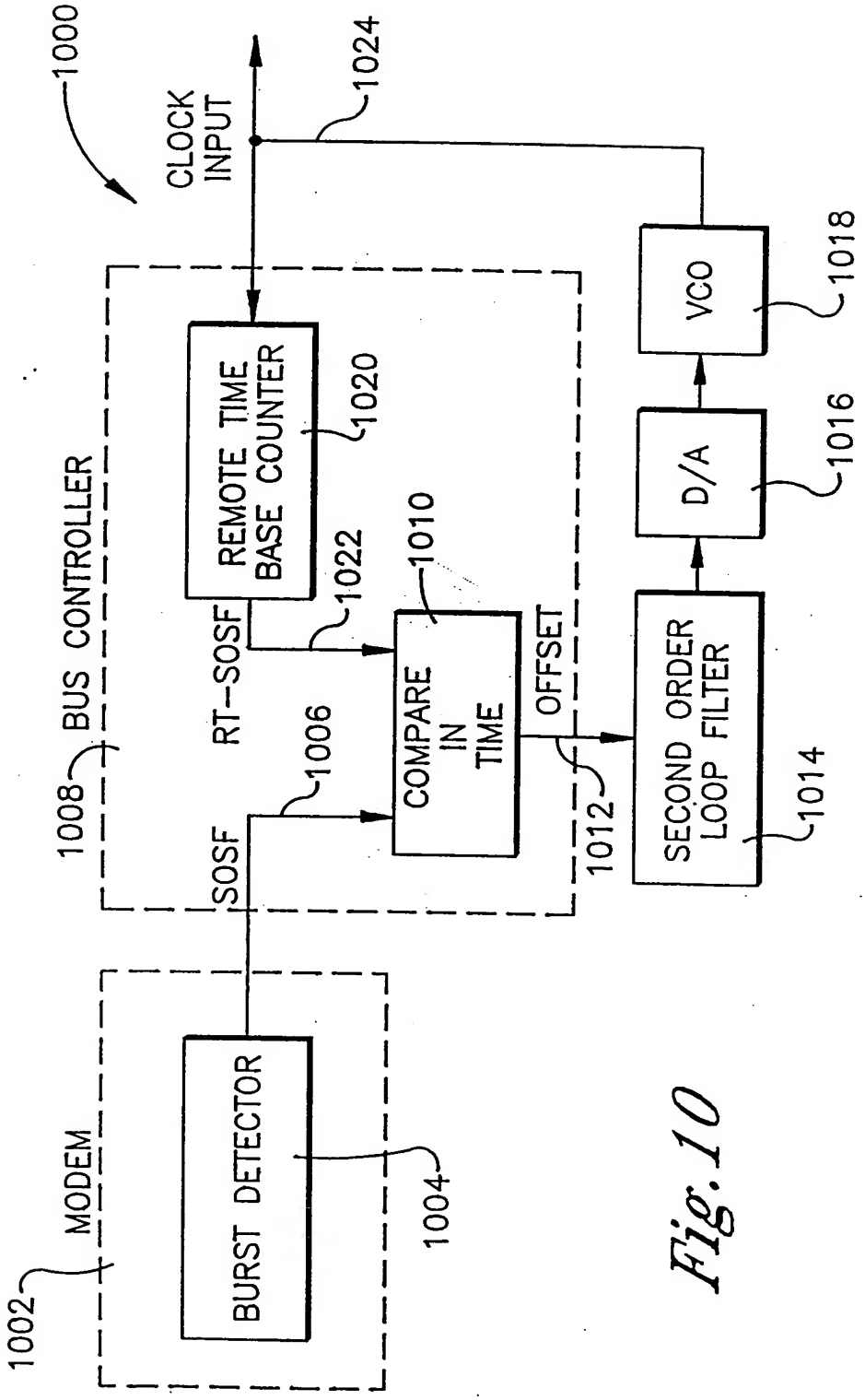

1000
CLOCK INPUT
1024
BUS CONTROLLER
1008
REMOTE TIME BASE COUNTER
1020
RT-SOSF
1022
1010
COMPARE IN TIME
OFFSET
1012
1006
SOSF
SECOND ORDER LOOP FILTER
1014
D/A
1016
VCO
1018
MODEM
1002
BURST DETECTOR
1004

Fig. 10

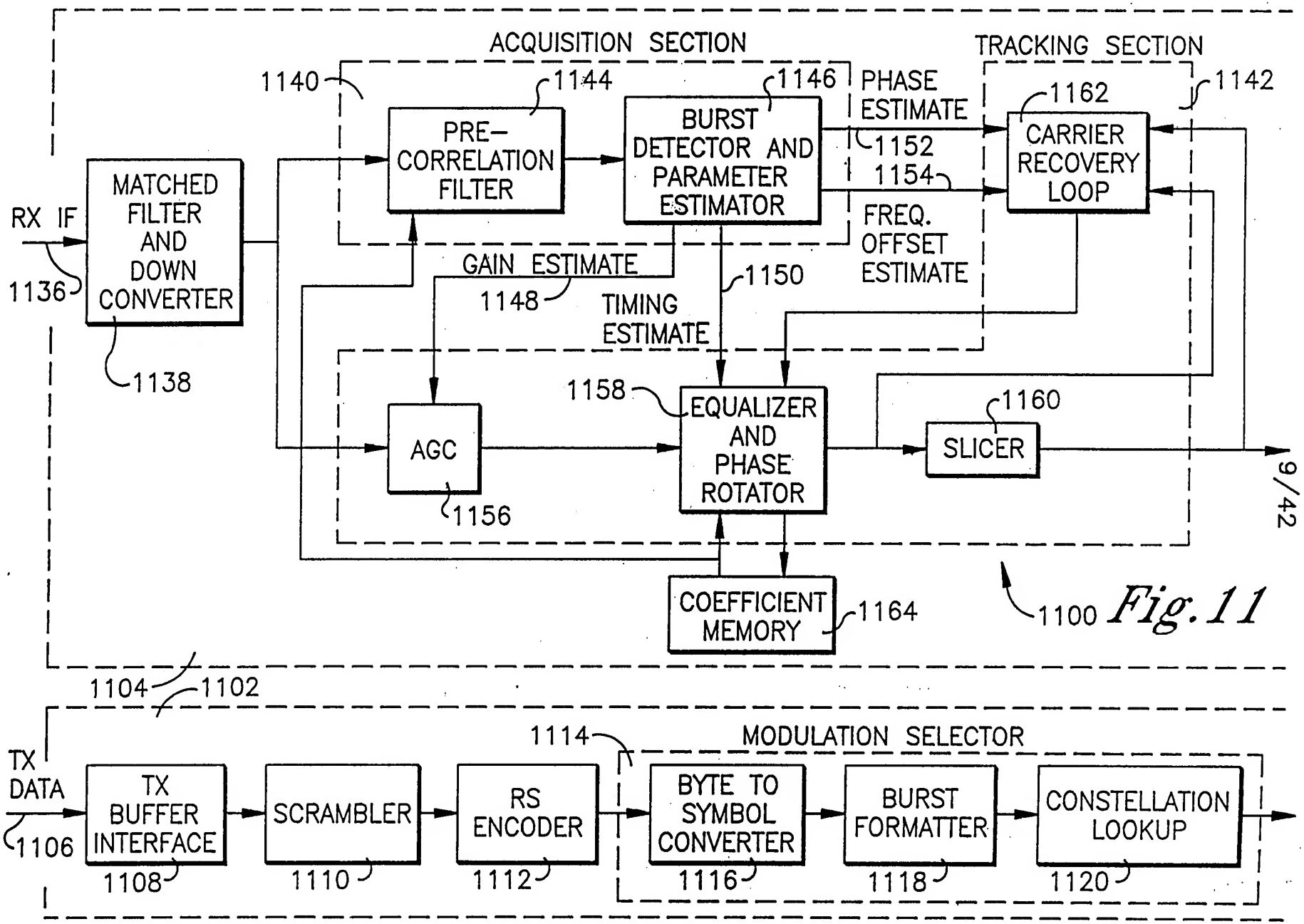
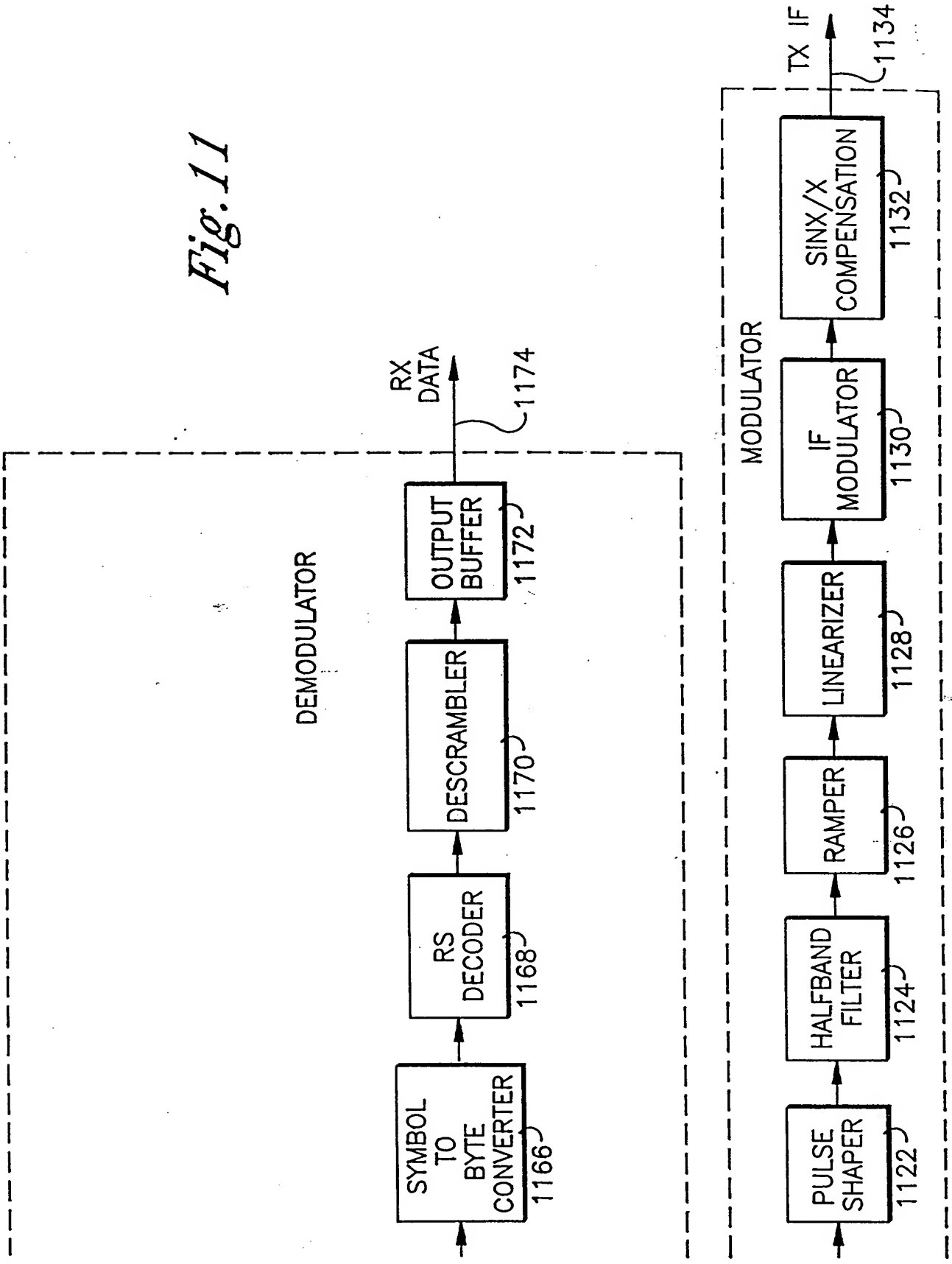

ACQUISITION SECTION
TRACKING SECTION
1140
1144
1146
1142
1162
PHASE ESTIMATE
PRE-CORRELATION FILTER
BURST DETECTOR AND PARAMETER ESTIMATOR
CARRIER RECOVERY LOOP
1152
1154
RX IF
MATCHED FILTER AND DOWN CONVERTER
FREQ. OFFSET ESTIMATE
GAIN ESTIMATE
1148
1150
1136
TIMING ESTIMATE
1138
1158
EQUALIZER AND PHASE ROTATOR
1160
AGC
SLICER
1156
9/42
COEFFICIENT MEMORY
1164
1100
1104
1102
1114
MODULATION SELECTOR
TX DATA
TX BUFFER INTERFACE
SCRAMBLER
RS ENCODER
BYTE TO SYMBOL CONVERTER
BURST FORMATTER
CONSTELLATION LOOKUP
1106
1108
1110
1112
1116
1118
1120

Fig. 11

Fig. 11


DEMODULATOR
SYMBOL TO BYTE CONVERTER
1166
RS DECODER
1168
DESCRAMBLER
1170
OUTPUT BUFFER
1172
RX DATA
1174
MODULATOR
PULSE SHAPER
1122
HALFBAND FILTER
1124
RAMPER
1126
LINEARIZER
1128
IF MODULATOR
1130
SINX/X COMPENSATION
1132
TX IF
1134

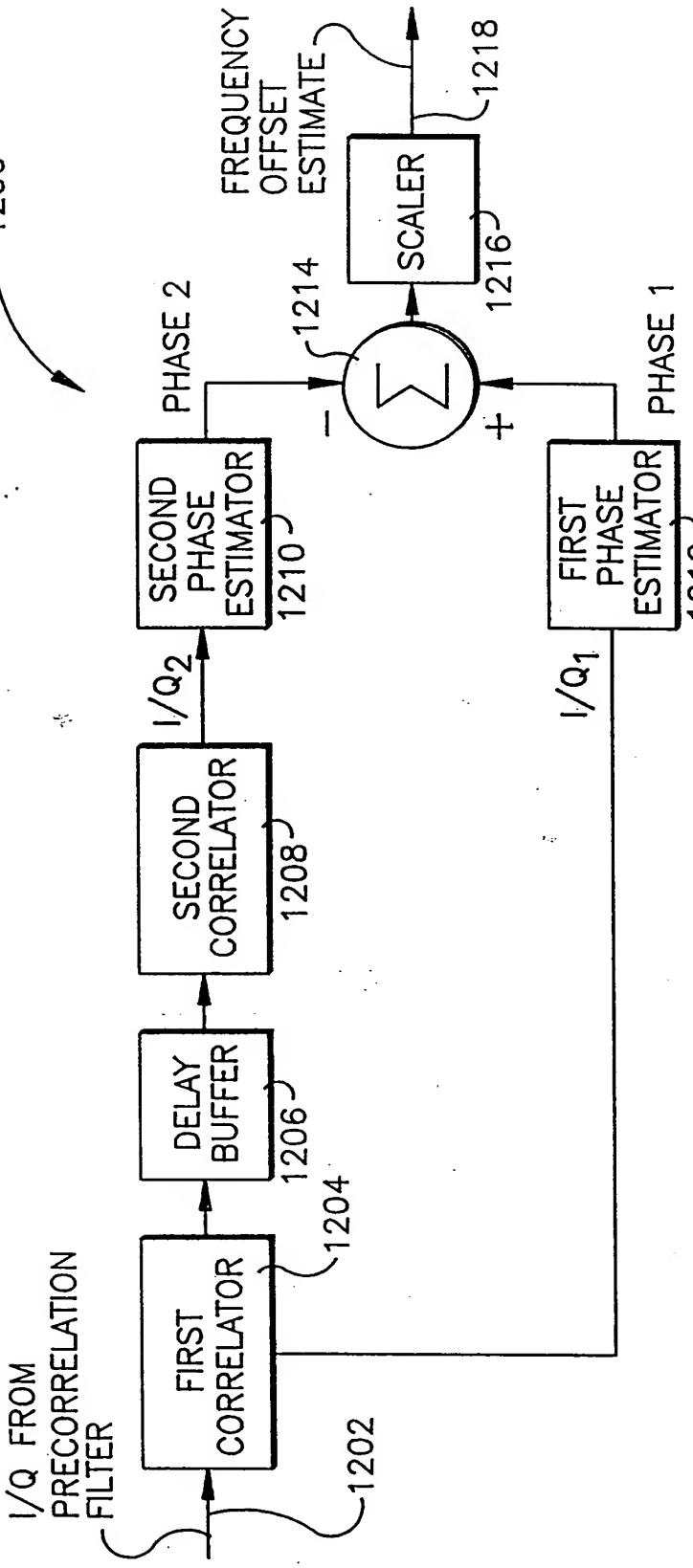

1200
I/Q FROM PRECORRELATION FILTER
FIRST CORRELATOR
1202
1204
DELAY BUFFER
1206
SECOND CORRELATOR
1208
I/Q2
SECOND PHASE ESTIMATOR
1210
PHASE 2
I/Q1
FIRST PHASE ESTIMATOR
1212
PHASE 1
1214
SCALER
1216
FREQUENCY OFFSET ESTIMATE
1218

Fig. 12

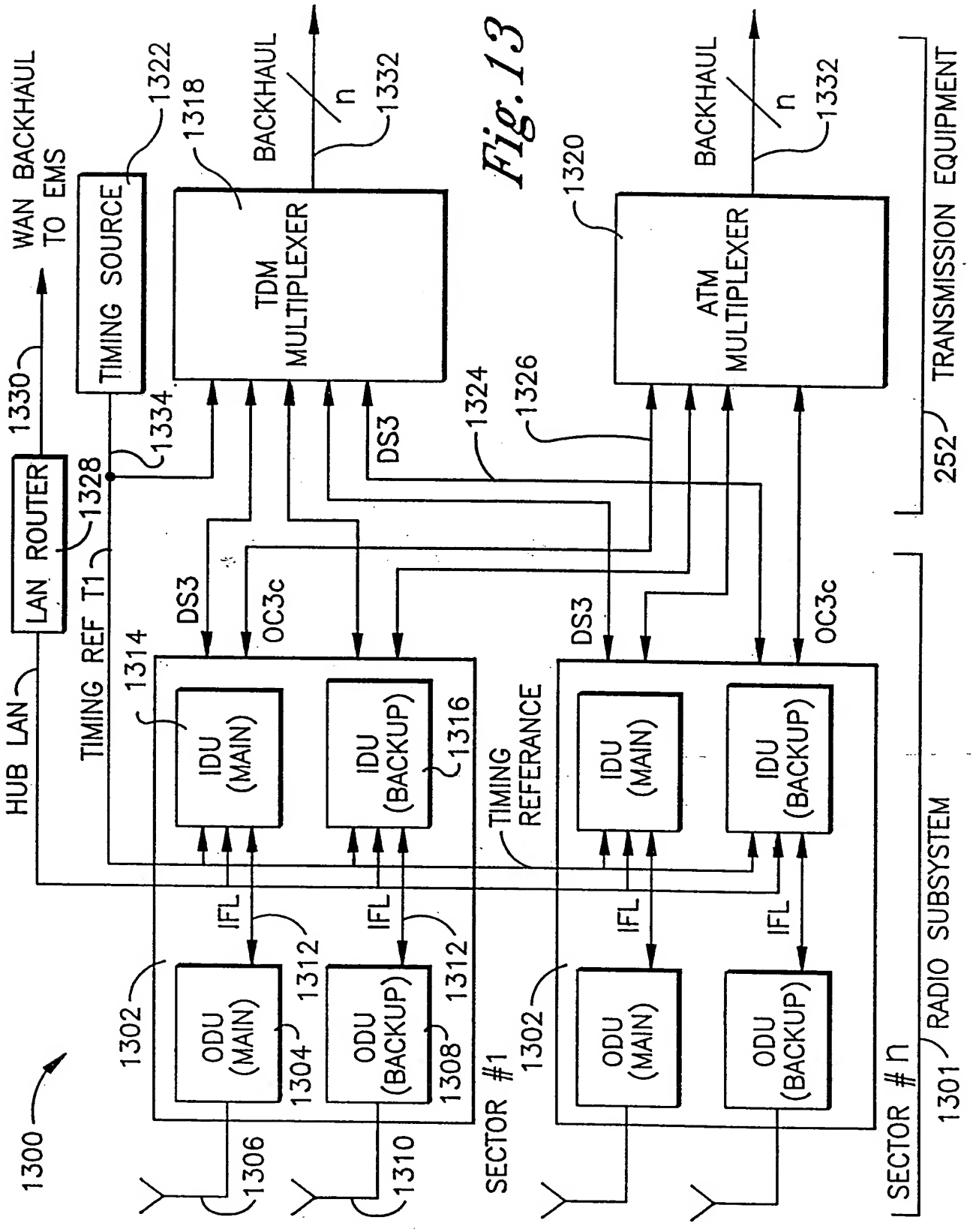

1300
HUB LAN
LAN ROUTER
1328
1330
WAN BACKHAUL
TO EMS
TIMING REF T1
TIMING SOURCE
1322
1334
TDM
MULTIPLEXER
1318
BACKHAUL
n
1332
DS3
1324
1326
ATM
MULTIPLEXER
1320
BACKHAUL
n
1332
252
TRANSMISSION EQUIPMENT
DS3
OC3c
DS3
OC3c
1314
IDU
(MAIN)
IDU
(BACKUP)
1316
TIMING
REFERANCE
IDU
(MAIN)
IDU
(BACKUP)
IFL
IFL
IFL
IFL
1302
ODU
(MAIN)
1304
1312
ODU
(BACKUP)
1308
1312
1302
ODU
(MAIN)
ODU
(BACKUP)
1306
1310
SECTOR #1
SECTOR #n
1301
RADIO SUBSYSTEM

Fig. 13

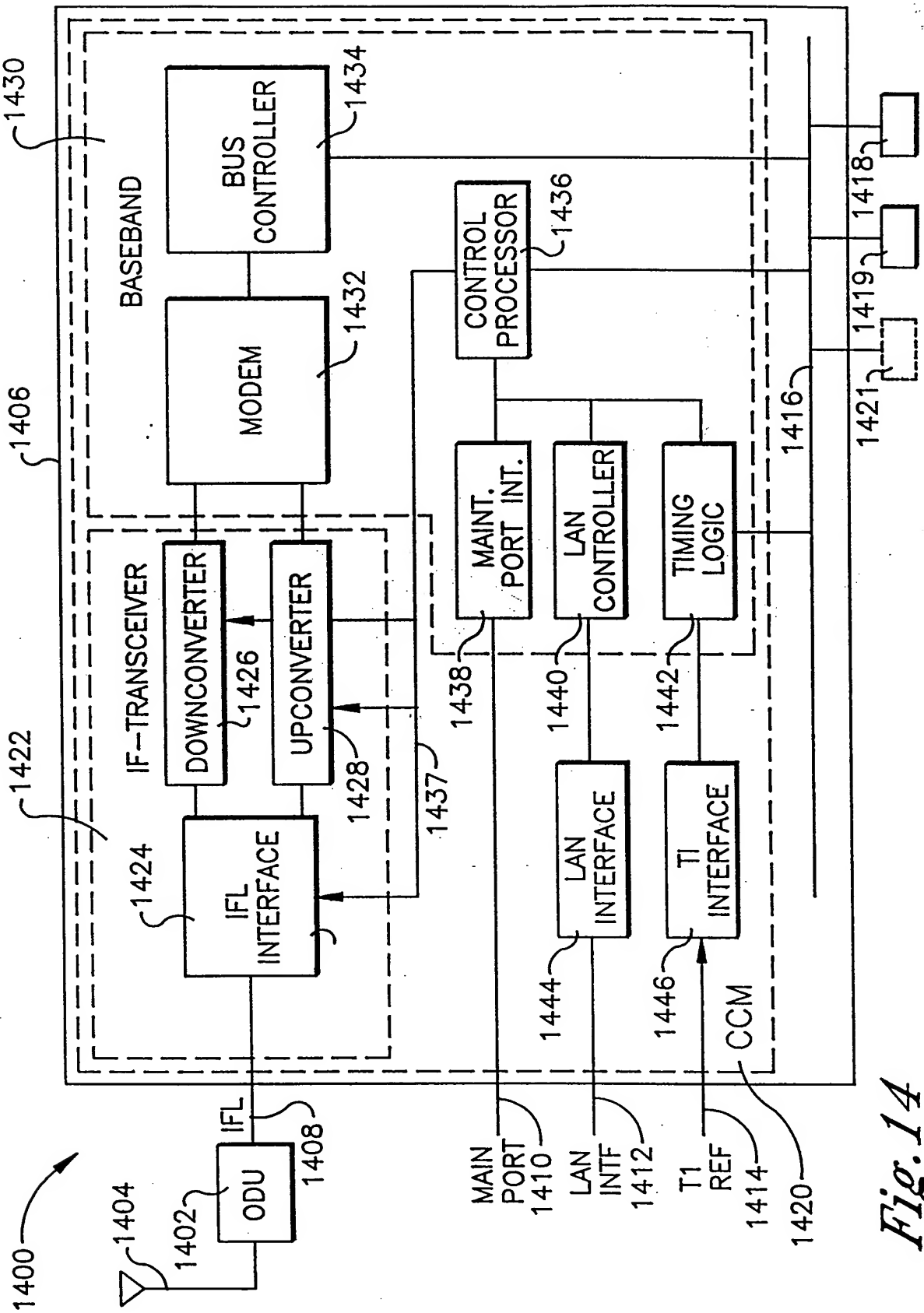

1400
1404
1402
ODU
IFL
1408
1406
1422
1424
IFL INTERFACE
IF-TRANSCEIVER
DOWNCONVERTER
1426
UPCONVERTER
1428
1437
1438
1440
1442
1444
1446
1430
BASEBAND
BUS CONTROLLER
1434
MODEM
1432
CONTROL PROCESSOR
1436
MAINT. PORT INT.
LAN CONTROLLER
TIMING LOGIC
LAN INTERFACE
TI INTERFACE
1416
1418
1419
1421
MAIN PORT 1410
LAN INTF 1412
T1 REF 1414
CCM
1420

Fig. 14

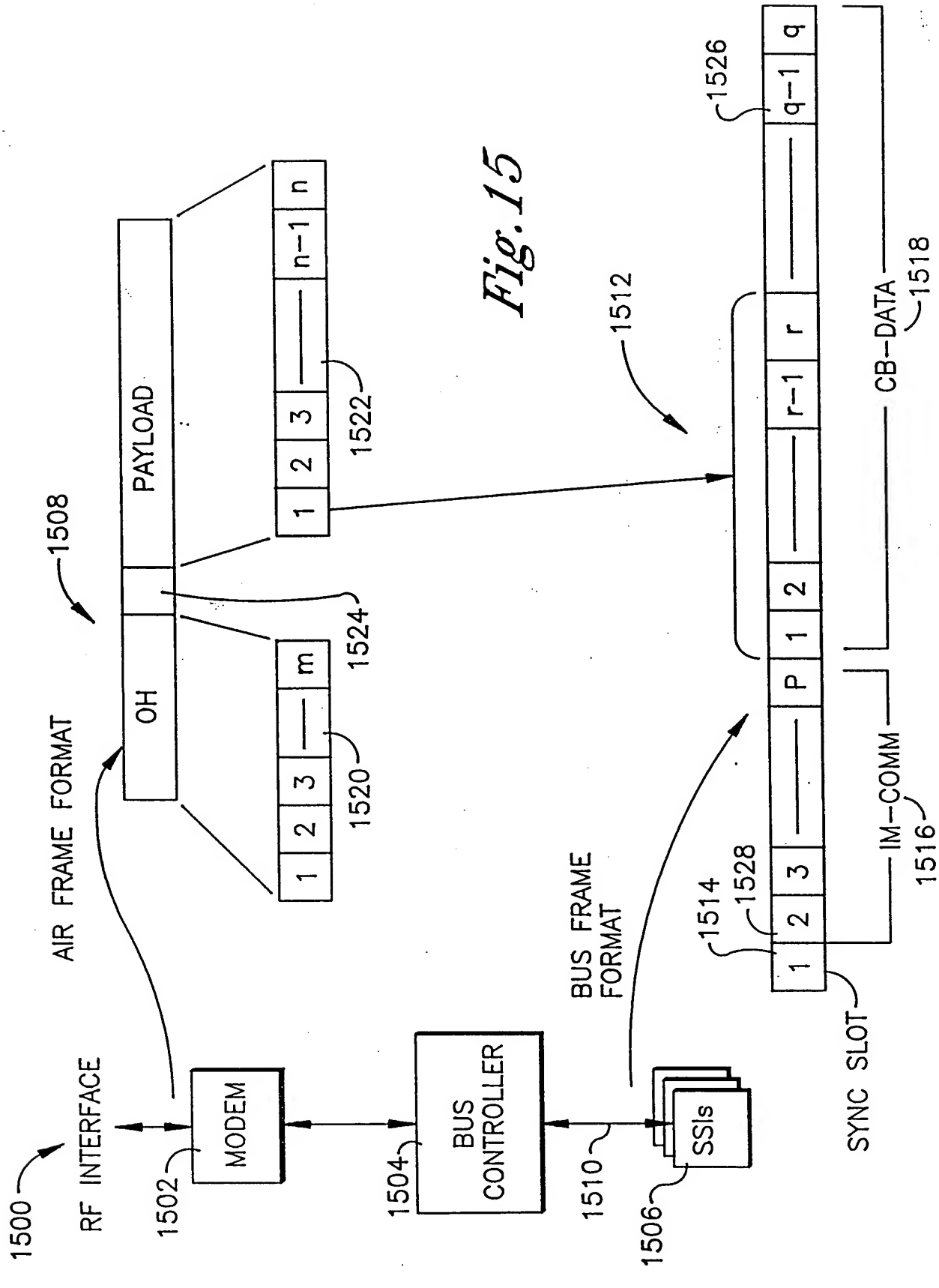

1500
RF INTERFACE
1502
MODEM
1504
BUS CONTROLLER
1506
SSIs
1508
AIR FRAME FORMAT
OH
PAYLOAD
1510
BUS FRAME FORMAT
1512
1514
1516
IM-COMM
1518
CB-DATA
1520
1522
1524
1526
1528
SYNC SLOT
1
2
3
m
n-1
n
P
r-1
r
q-1
q

Fig. 15

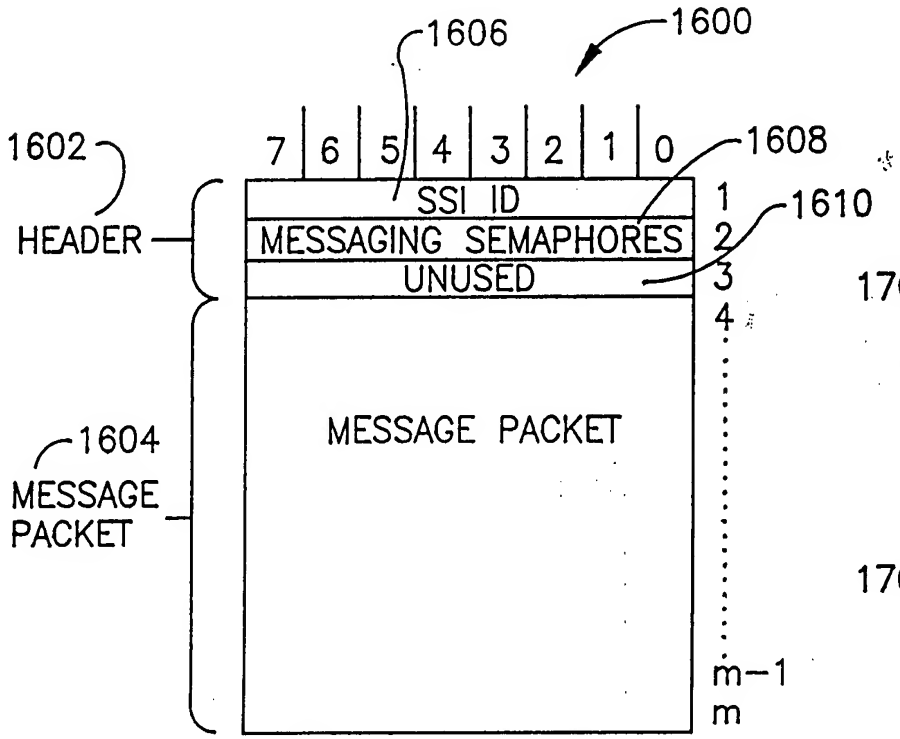

1606
1600
1602
7 6 5 4 3 2 1 0
1608
SSI ID
1
HEADER
MESSAGING SEMAPHORES
2
1610
UNUSED
3
4
1604
MESSAGE PACKET
MESSAGE PACKET
m-1
m

Fig. 16

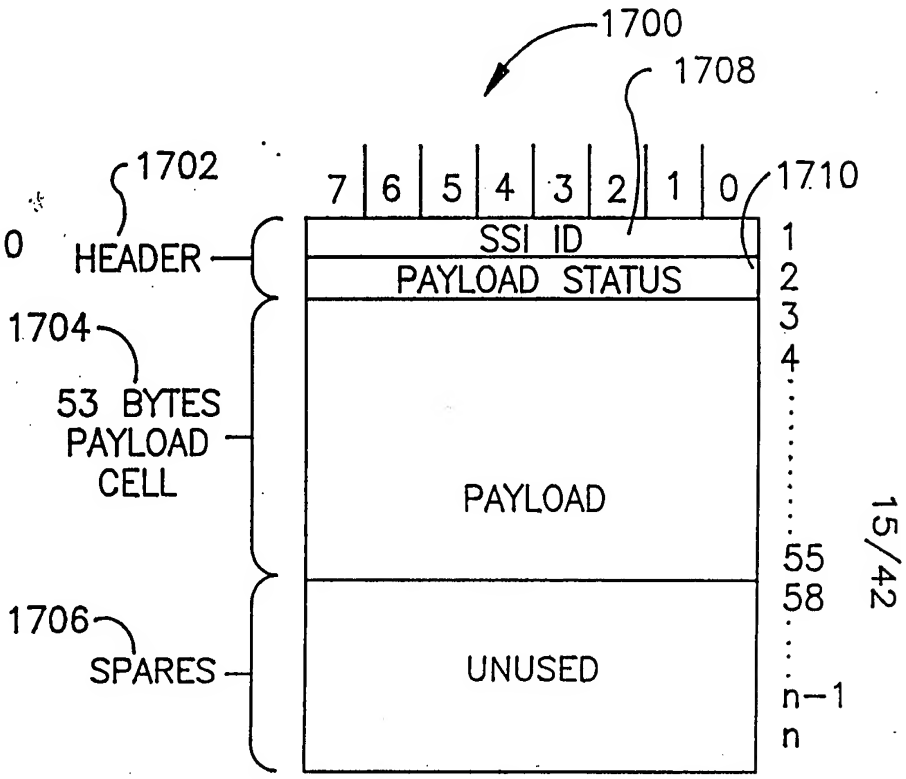

1700
1708
1702
7 6 5 4 3 2 1 0
1710
SSI ID
1
HEADER
PAYLOAD STATUS
2
3
1704
4
53 BYTES
PAYLOAD
CELL
PAYLOAD
55
58
1706
SPARES
UNUSED
n-1
n

Fig. 17

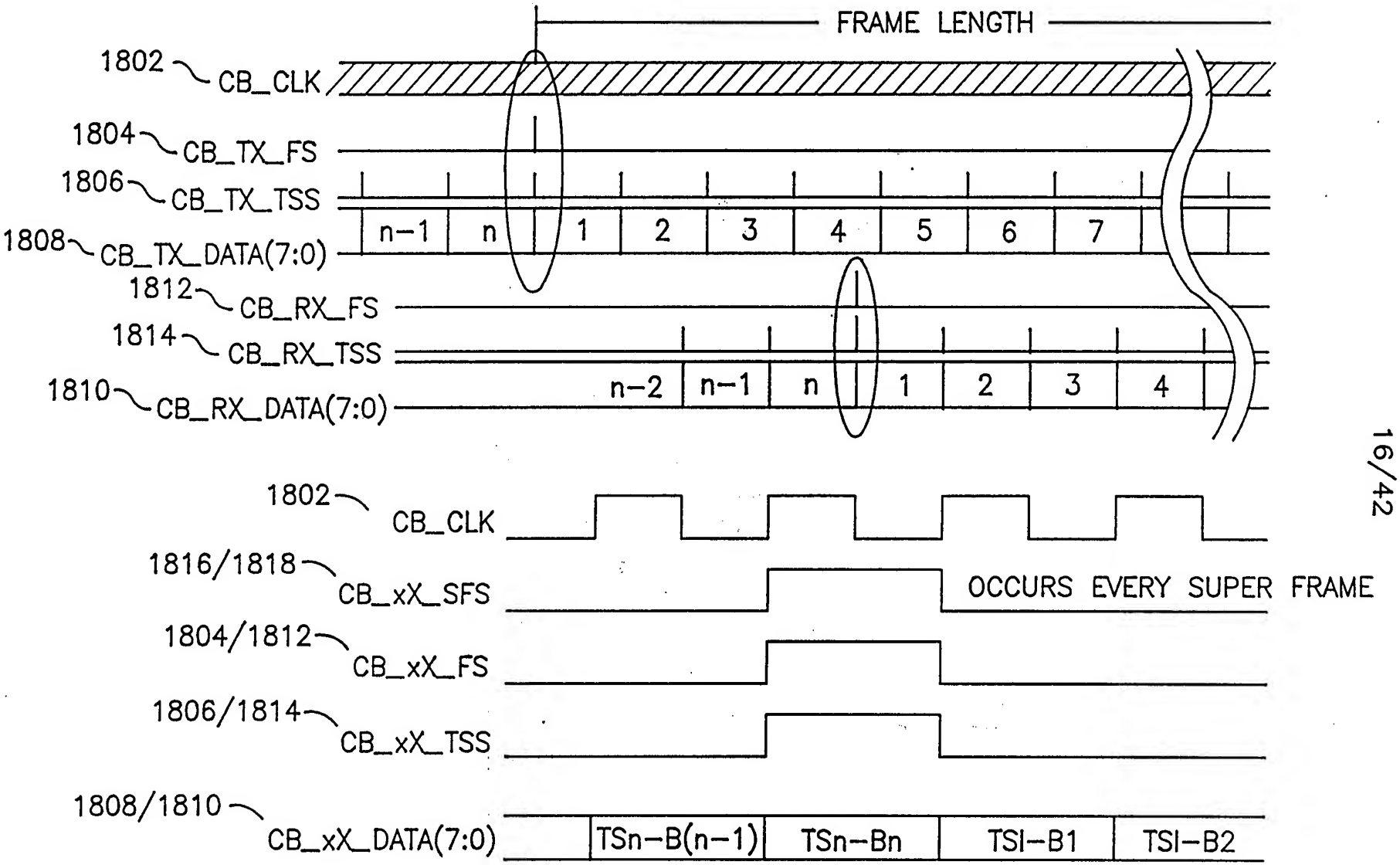


Fig. 18 CELL BUS TIMING

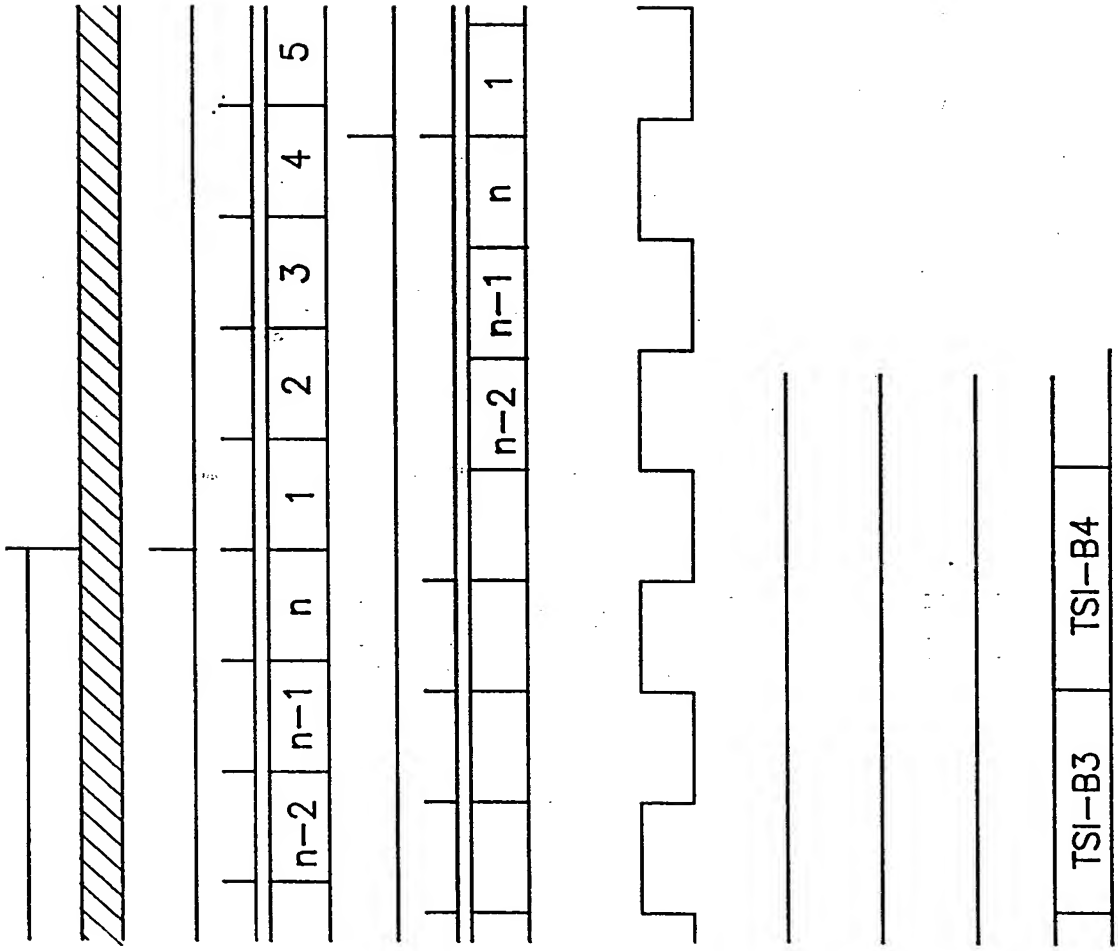


Fig. 18

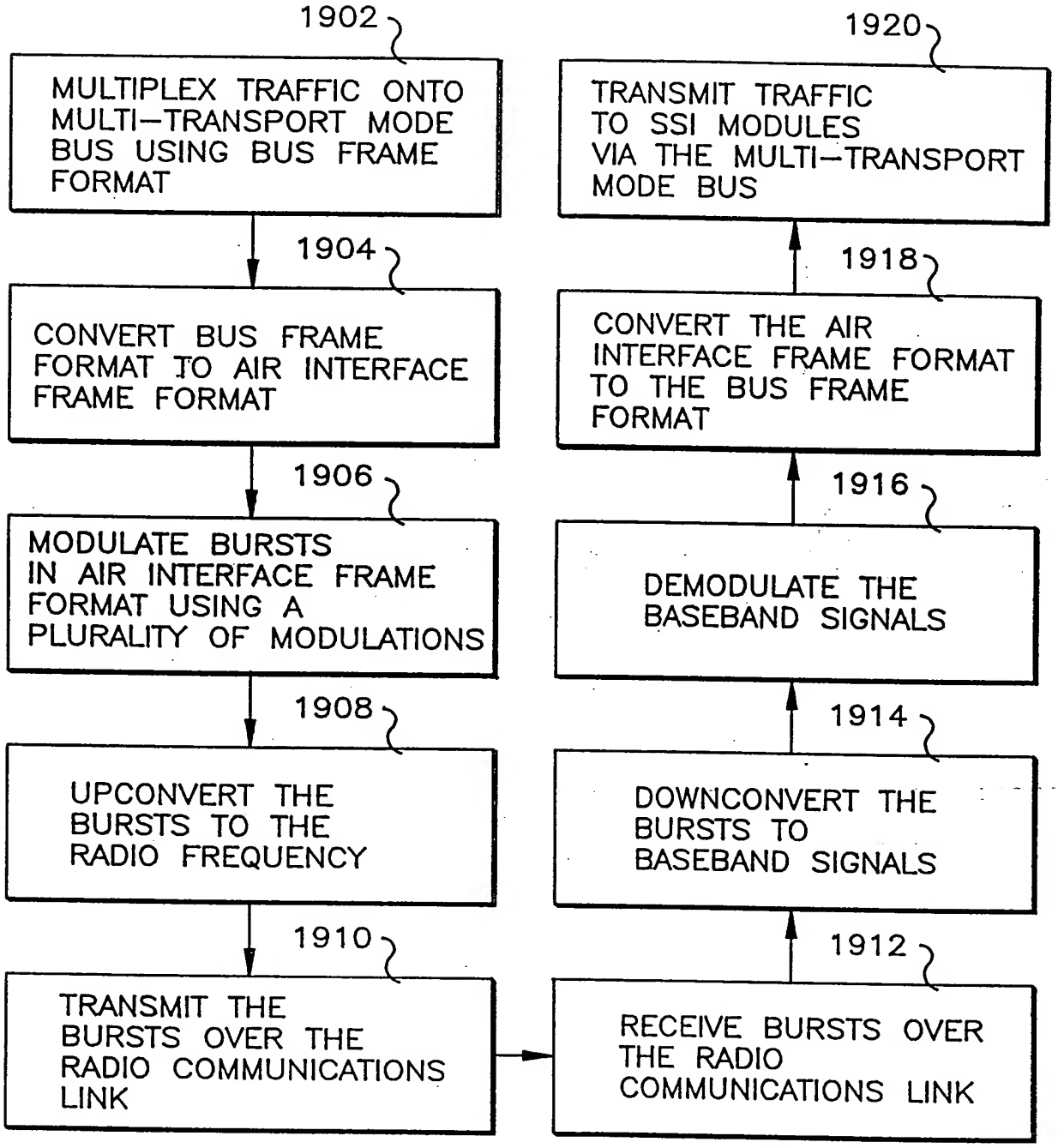

1902
MULTIPLEX TRAFFIC ONTO MULTI–TRANSPORT MODE BUS USING BUS FRAME FORMAT
1904
CONVERT BUS FRAME FORMAT TO AIR INTERFACE FRAME FORMAT
1906
MODULATE BURSTS IN AIR INTERFACE FRAME FORMAT USING A PLURALITY OF MODULATIONS
1908
UPCONVERT THE BURSTS TO THE RADIO FREQUENCY
1910
TRANSMIT THE BURSTS OVER THE RADIO COMMUNICATIONS LINK
1912
RECEIVE BURSTS OVER THE RADIO COMMUNICATIONS LINK
1914
DOWNCONVERT THE BURSTS TO BASEBAND SIGNALS
1916
DEMODULATE THE BASEBAND SIGNALS
1918
CONVERT THE AIR INTERFACE FRAME FORMAT TO THE BUS FRAME FORMAT
1920
TRANSMIT TRAFFIC TO SSI MODULES VIA THE MULTI–TRANSPORT MODE BUS

Fig. 19

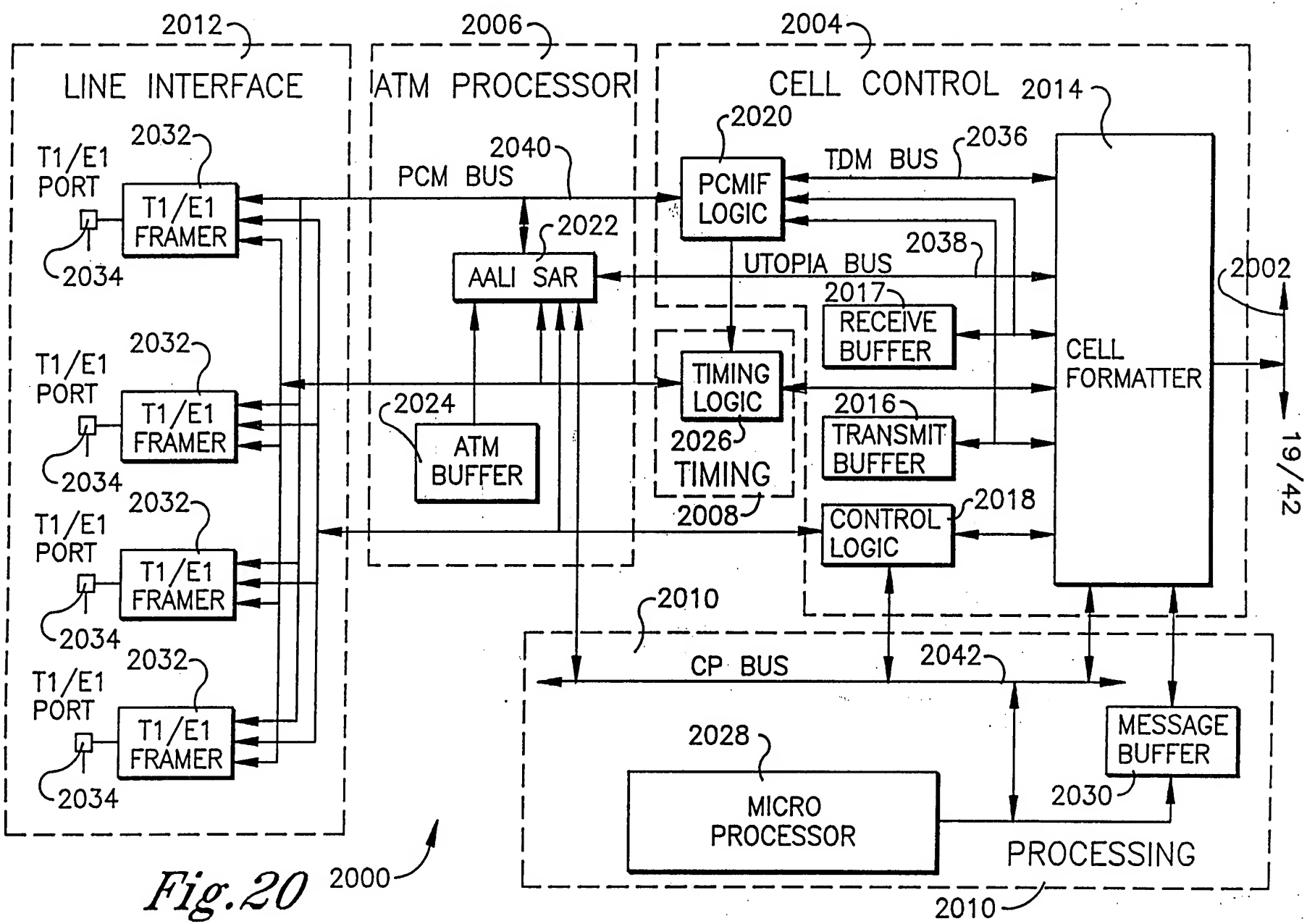

2012
LINE INTERFACE
2006
ATM PROCESSOR
2004
CELL CONTROL
2014
T1/E1 PORT
2032
T1/E1 FRAMER
2034
2040
PCM BUS
2022
AALI SAR
2020
PCMIF LOGIC
TDM BUS
2036
2038
UTOPIA BUS
2017
RECEIVE BUFFER
2002
CELL FORMATTER
TIMING LOGIC
2024
ATM BUFFER
2026
TIMING
2008
2016
TRANSMIT BUFFER
2018
CONTROL LOGIC
2010
CP BUS
2042
2028
MICRO PROCESSOR
MESSAGE BUFFER
2030
PROCESSING
2010
2000
19/42

Fig. 20

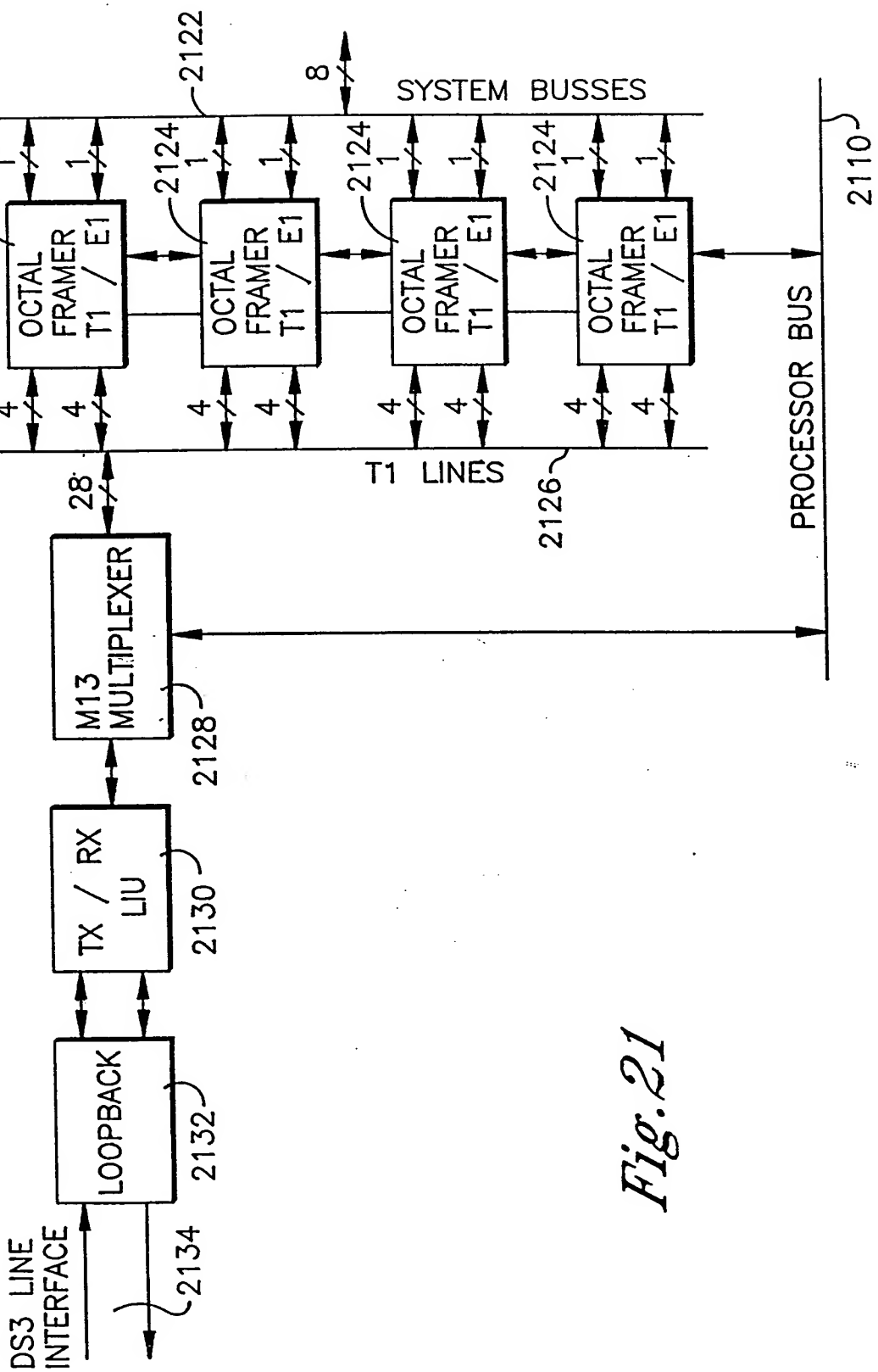

2122
8
SYSTEM BUSSES
2124
1
OCTAL FRAMER T1 / E1
4
T1 LINES
2126
28
2110
PROCESSOR BUS
M13 MULTIPLEXER
2128
TX / RX LIU
2130
LOOPBACK
2132
2134
DS3 LINE INTERFACE

Fig. 21

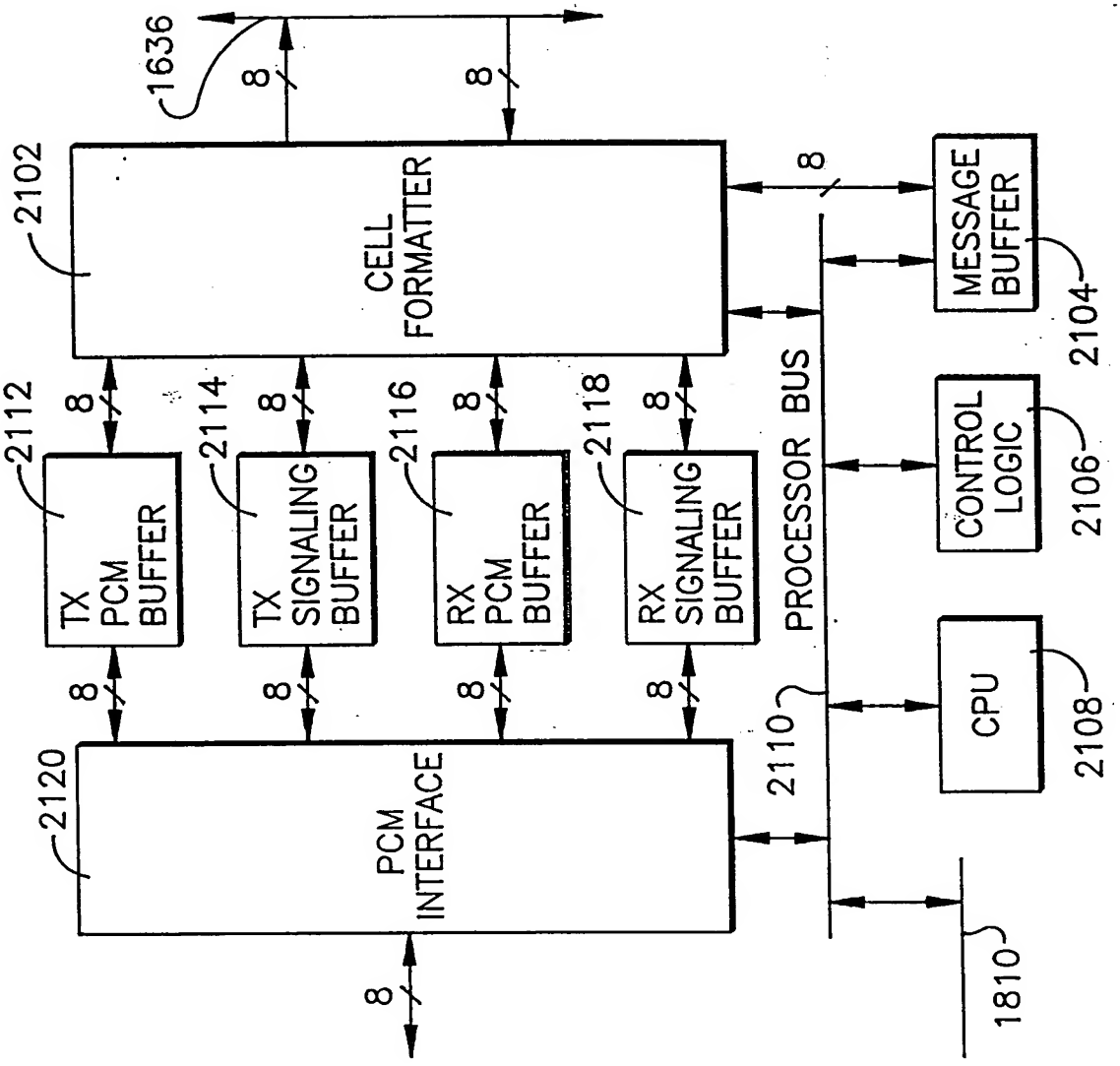

1636
8
8
2102
CELL FORMATTER
8
MESSAGE BUFFER
2104
2112
TX PCM BUFFER
2114
TX SIGNALING BUFFER
2116
RX PCM BUFFER
2118
RX SIGNALING BUFFER
PROCESSOR BUS
CONTROL LOGIC
2106
CPU
2108
2110
2120
PCM INTERFACE
1810

Fig. 21

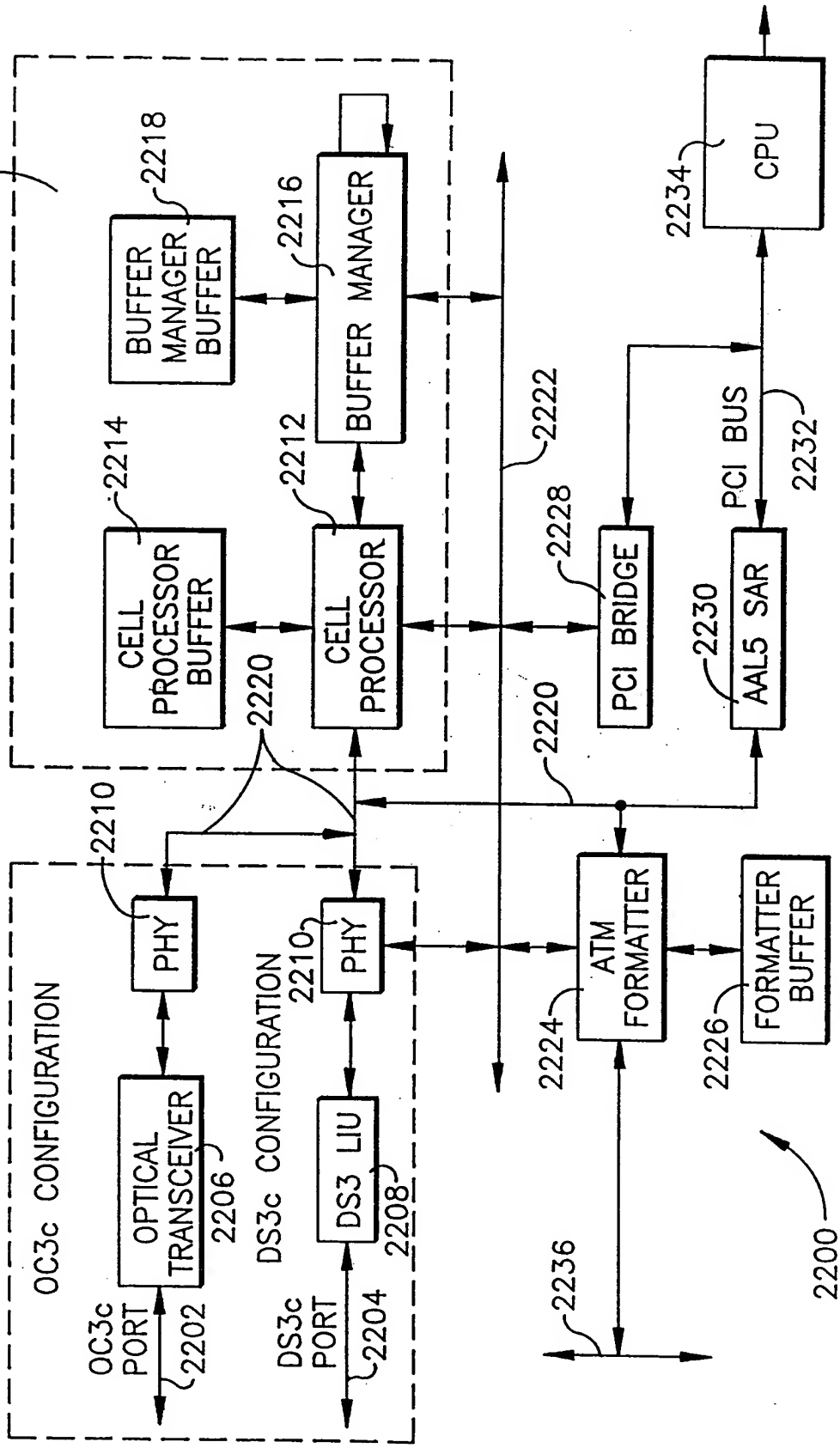

2211
2218
BUFFER MANAGER BUFFER
2216
BUFFER MANAGER
2234
CPU
2214
CELL PROCESSOR BUFFER
2212
CELL PROCESSOR
2222
2228
PCI BRIDGE
PCI BUS
2232
2230
AAL5 SAR
2220
2220
2210
OC3c CONFIGURATION
PHY
2210
PHY
DS3c CONFIGURATION
ATM FORMATTER
FORMATTER BUFFER
2224
2226
OPTICAL TRANSCEIVER
2206
DS3 LIU
2208
OC3c PORT
2202
DS3c PORT
2204
2236
2200

Fig. 22

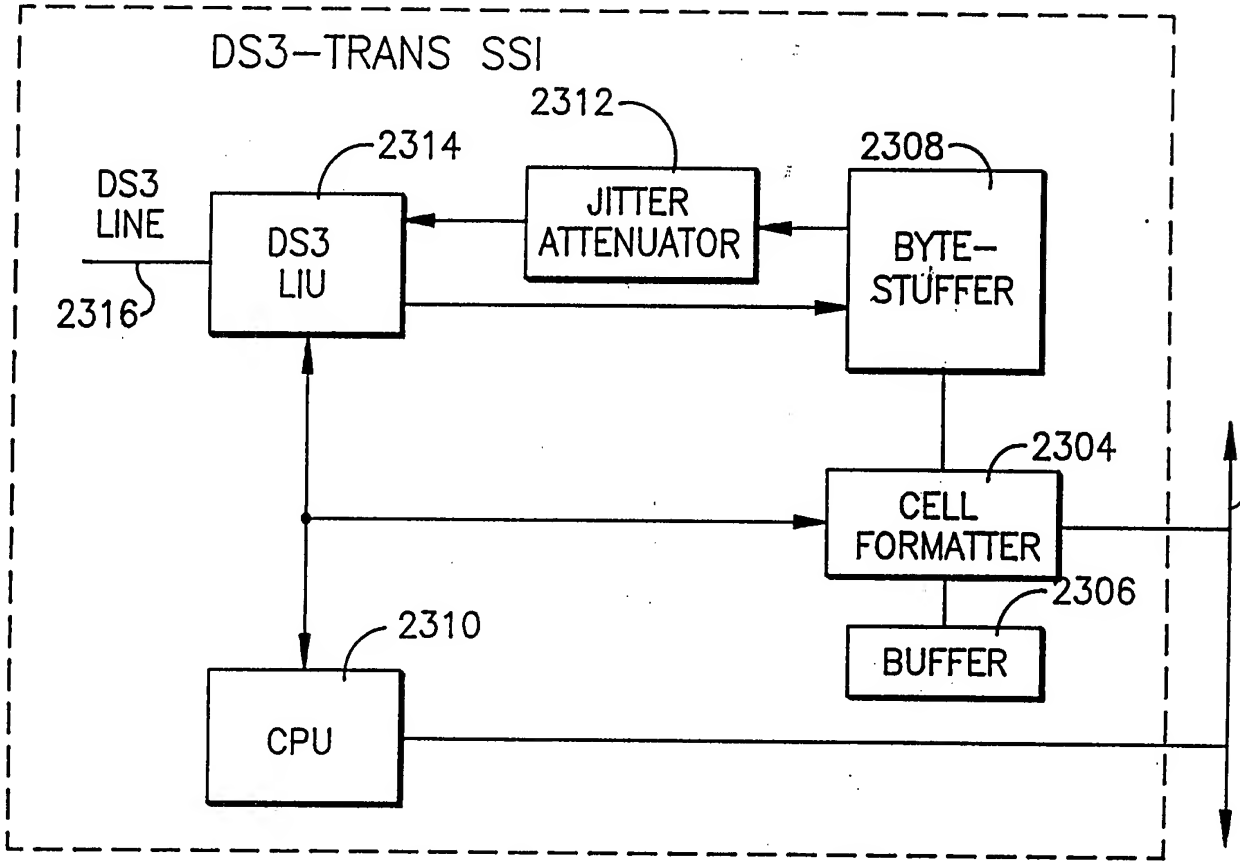

DS3–TRANS SSI
2312
2314
2308
2300
DS3
LINE
JITTER
ATTENUATOR
DS3
LIU
BYTE–
STUFFER
2316
2304
2302
CELL
FORMATTER
2306
2310
BUFFER
CPU

Fig.23

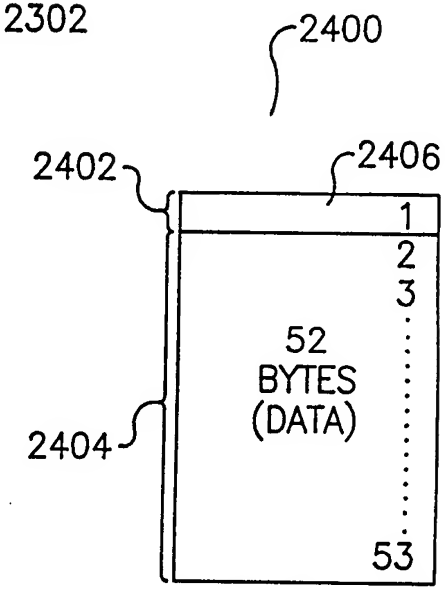

2400
2402
2406
1
2
3
52
BYTES
(DATA)
53
2404

Fig.24

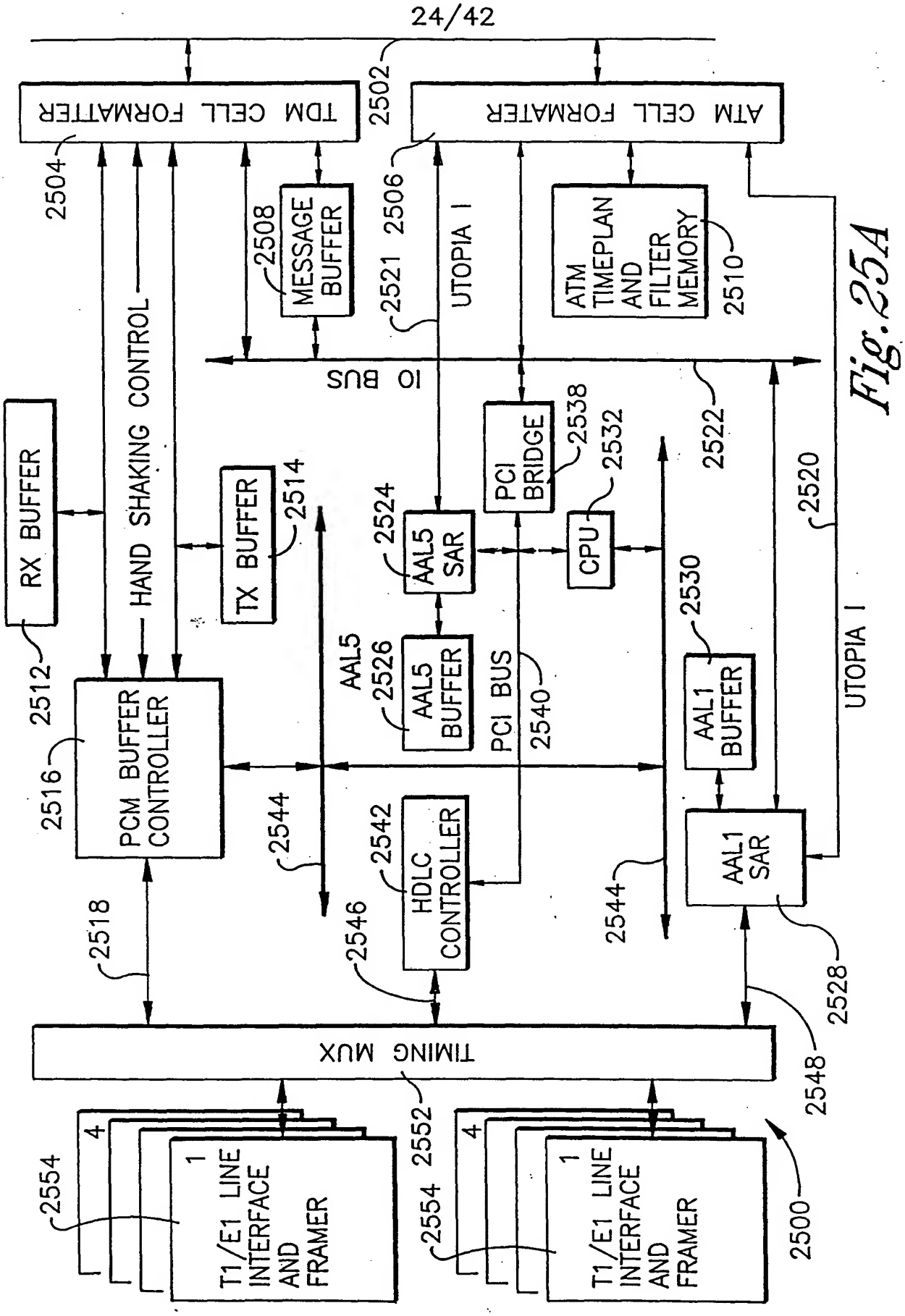

TDM CELL FORMATTER
ATM CELL FORMATTER
2502
2504
2506
2508
MESSAGE BUFFER
2521
UTOPIA I
ATM TIMEPLAN AND FILTER MEMORY
2510
TO BUS
2522
RX BUFFER
HAND SHAKING CONTROL
TX BUFFER
2514
PCI BRIDGE
2538
2532
2524
AAL5 SAR
CPU
2520
2530
AAL5
2526
AAL5 BUFFER
PCI BUS
2540
AAL1 BUFFER
UTOPIA I
2512
2516
PCM BUFFER CONTROLLER
2544
2542
HDLC CONTROLLER
AAL1 SAR
2518
2546
2528
TIMING MUX
2548
2554
4
1
T1/E1 LINE INTERFACE AND FRAMER
2552
2500

Fig. 25A

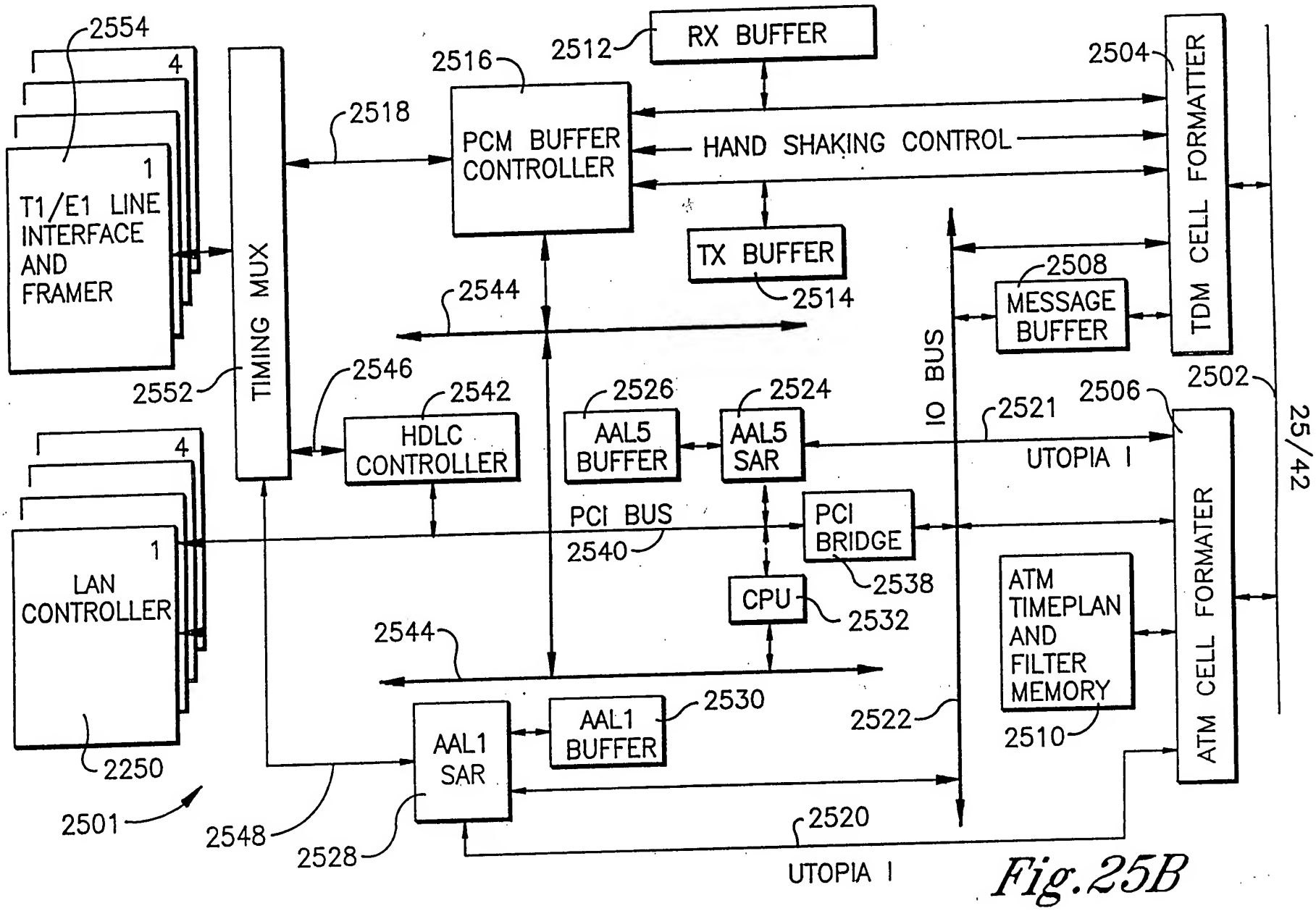

2554
4
1
T1/E1 LINE INTERFACE AND FRAMER
2552
TIMING MUX
2518
2516
PCM BUFFER CONTROLLER
2512
RX BUFFER
HAND SHAKING CONTROL
TX BUFFER
2514
2544
2504
TDM CELL FORMATTER
2508
MESSAGE BUFFER
IO BUS
2502
2506
2521
UTOPIA I
2546
2542
HDLC CONTROLLER
2526
AAL5 BUFFER
2524
AAL5 SAR
4
1
LAN CONTROLLER
2250
PCI BUS
2540
PCI BRIDGE
2538
CPU
2532
2544
2530
AAL1 BUFFER
AAL1 SAR
2522
ATM TIMEPLAN AND FILTER MEMORY
2510
ATM CELL FORMATER
2501
2548
2528
2520
UTOPIA I
25/42

Fig. 25B

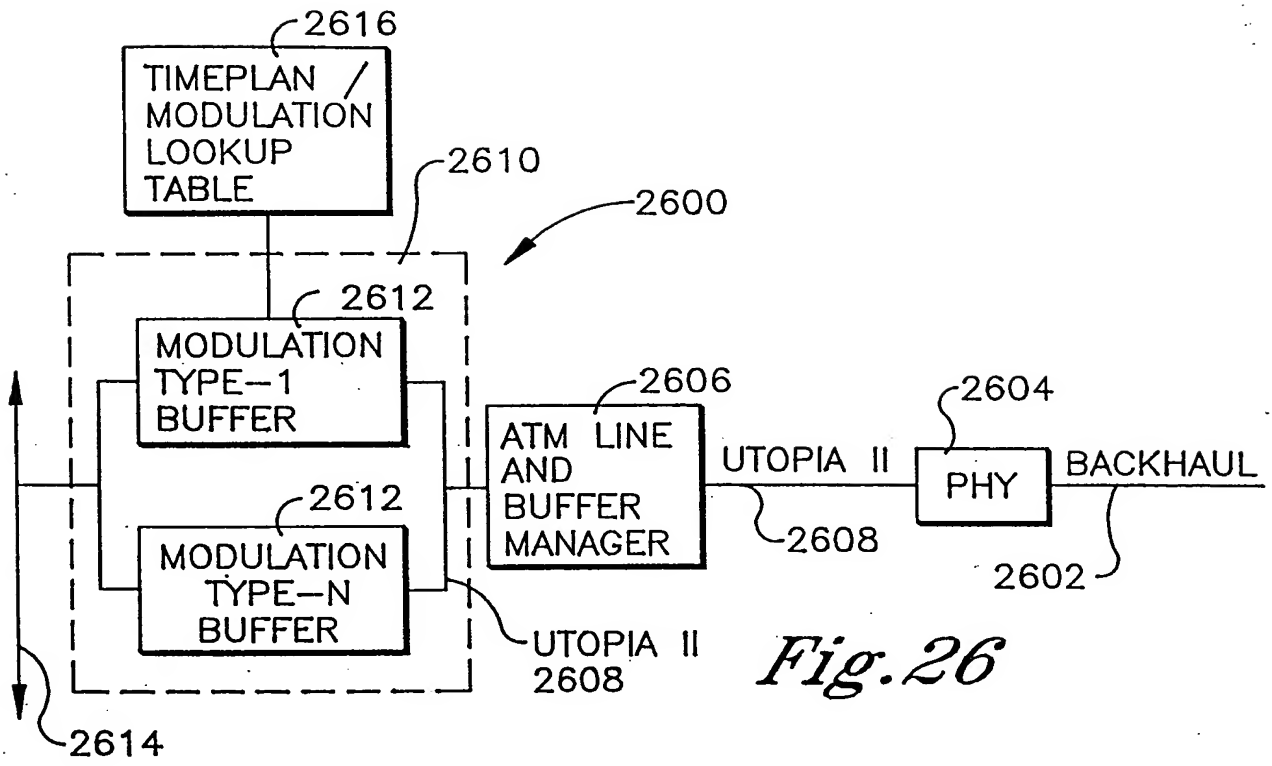
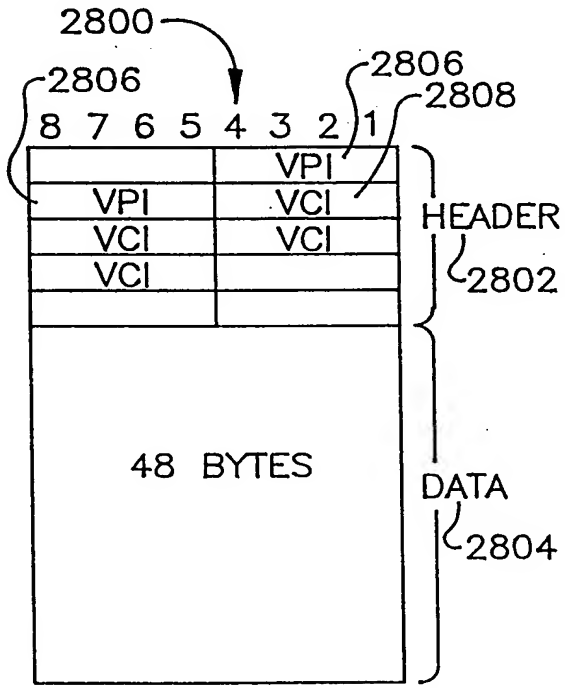
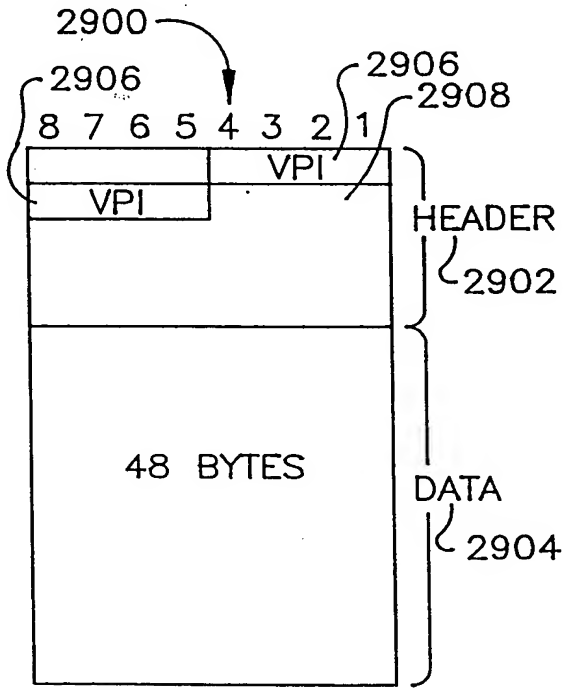


Fig. 26



ATM CELL

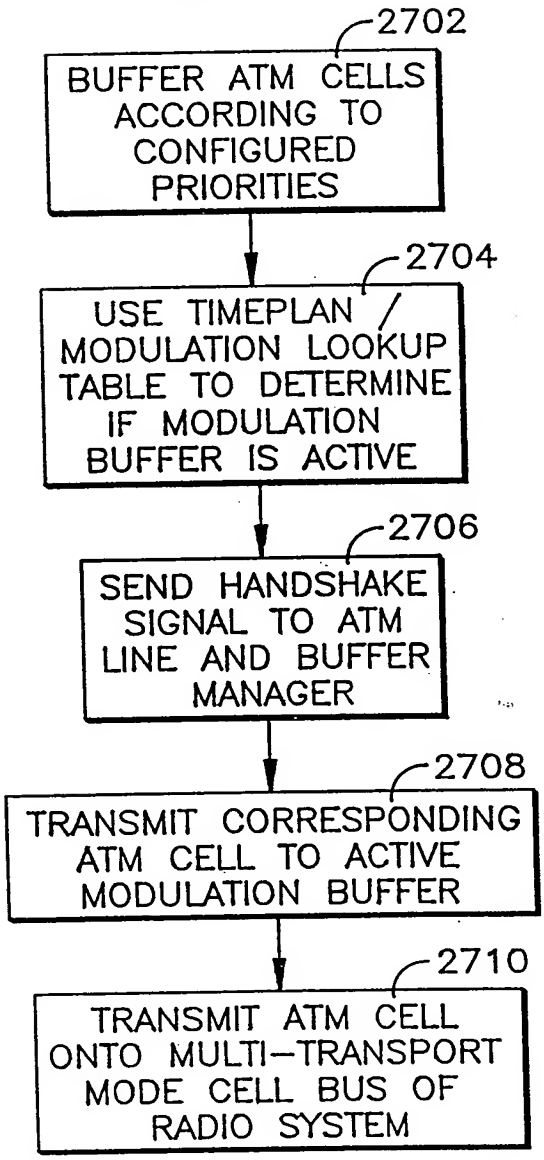
Fig. 28



TDM CELL

Fig. 29

Fig. 27


2702
BUFFER ATM CELLS ACCORDING TO CONFIGURED PRIORITIES
2704
USE TIMEPLAN / MODULATION LOOKUP TABLE TO DETERMINE IF MODULATION BUFFER IS ACTIVE
2706
SEND HANDSHAKE SIGNAL TO ATM LINE AND BUFFER MANAGER
2708
TRANSMIT CORRESPONDING ATM CELL TO ACTIVE MODULATION BUFFER
2710
TRANSMIT ATM CELL ONTO MULTI-TRANSPORT MODE CELL BUS OF RADIO SYSTEM

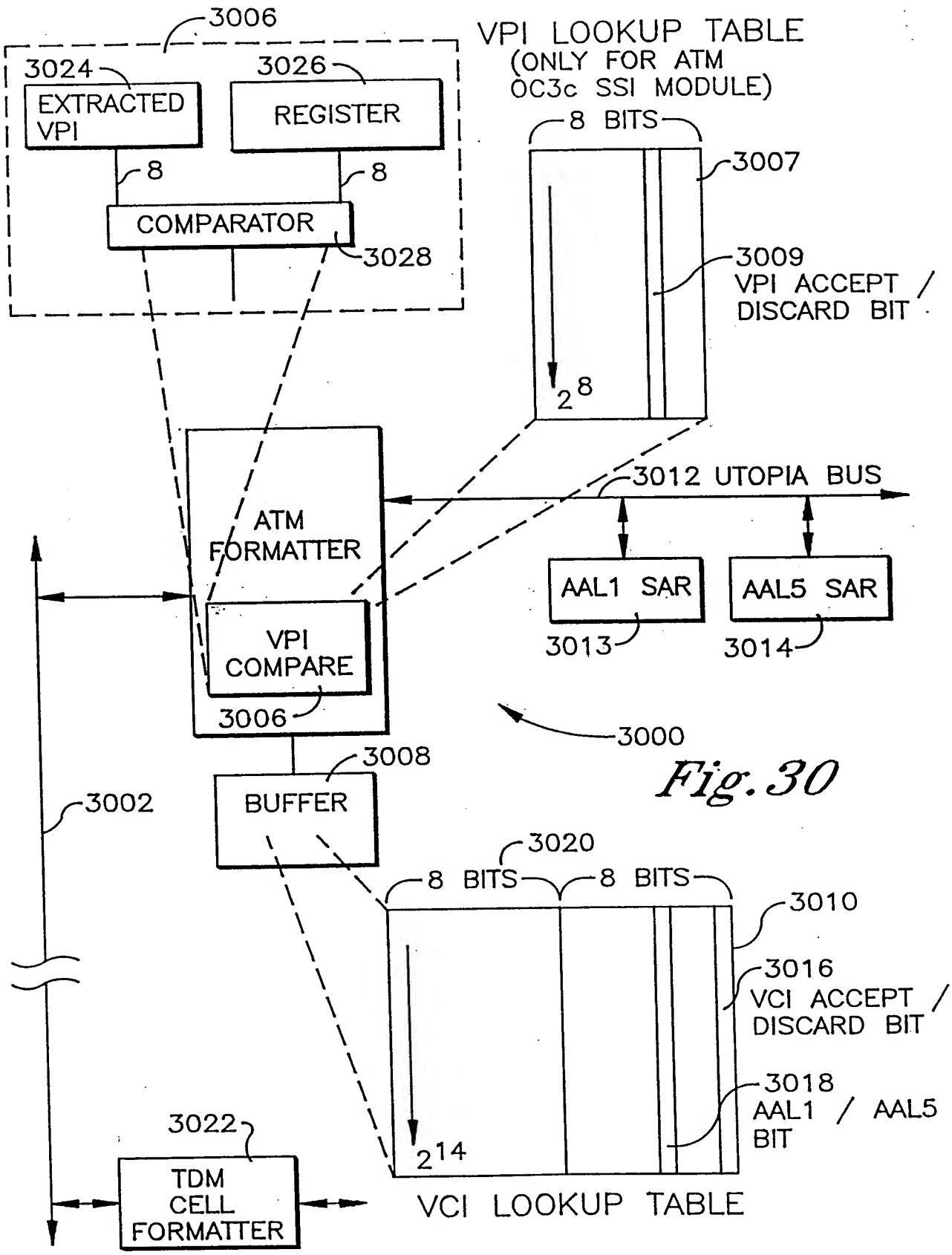

3006
3024
EXTRACTED VPI
3026
REGISTER
8
8
COMPARATOR
3028
VPI LOOKUP TABLE
(ONLY FOR ATM OC3c SSI MODULE)
8 BITS
3007
3009
VPI ACCEPT / DISCARD BIT
2 8
3012 UTOPIA BUS
ATM FORMATTER
VPI COMPARE
3006
AAL1 SAR
AAL5 SAR
3013
3014
3000
3008
BUFFER
3002
3020
8 BITS
8 BITS
3010
3016
VCI ACCEPT / DISCARD BIT
3018
AAL1 / AAL5 BIT
2 14
VCI LOOKUP TABLE
3022
TDM CELL FORMATTER

Fig. 30

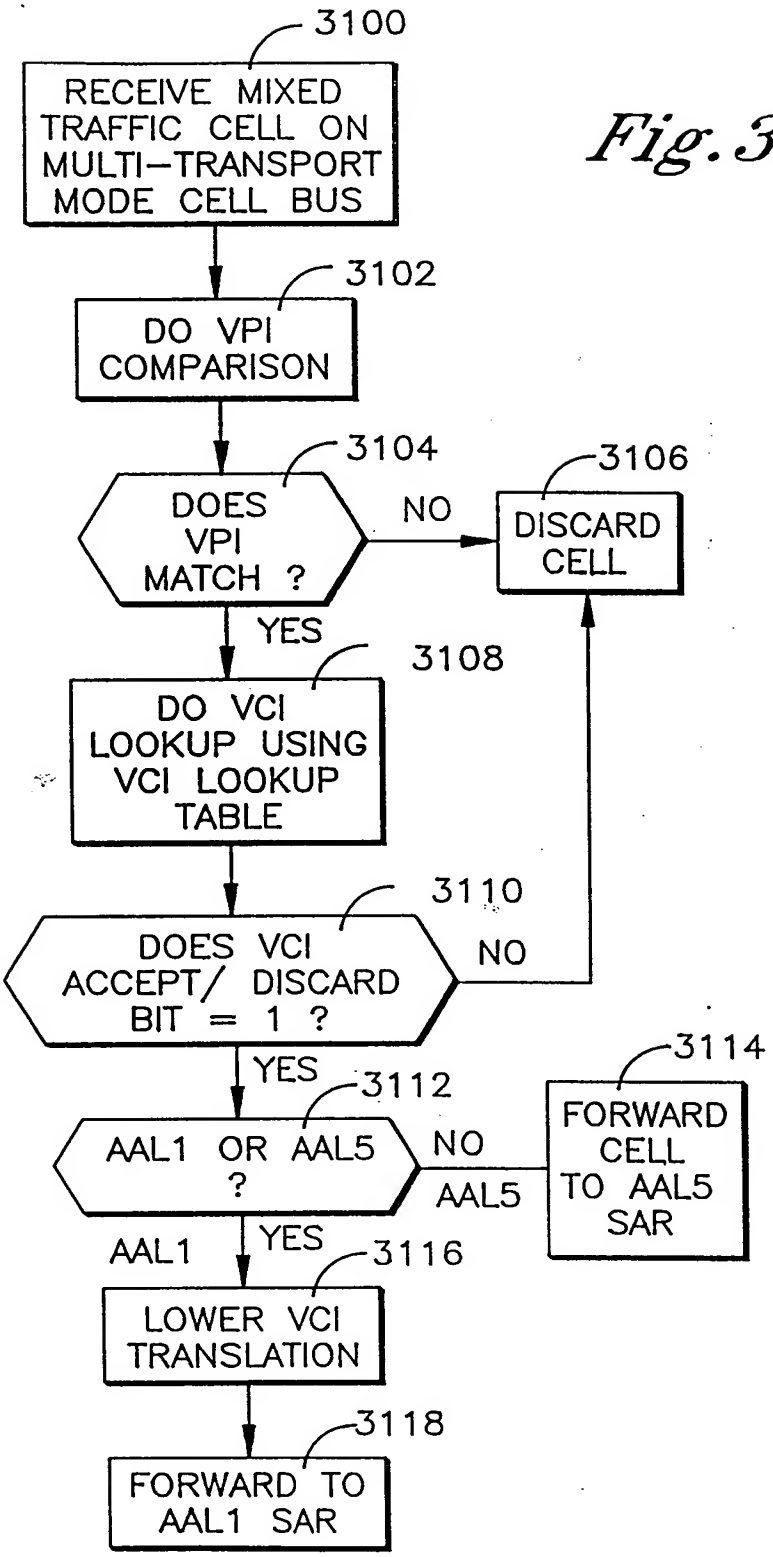
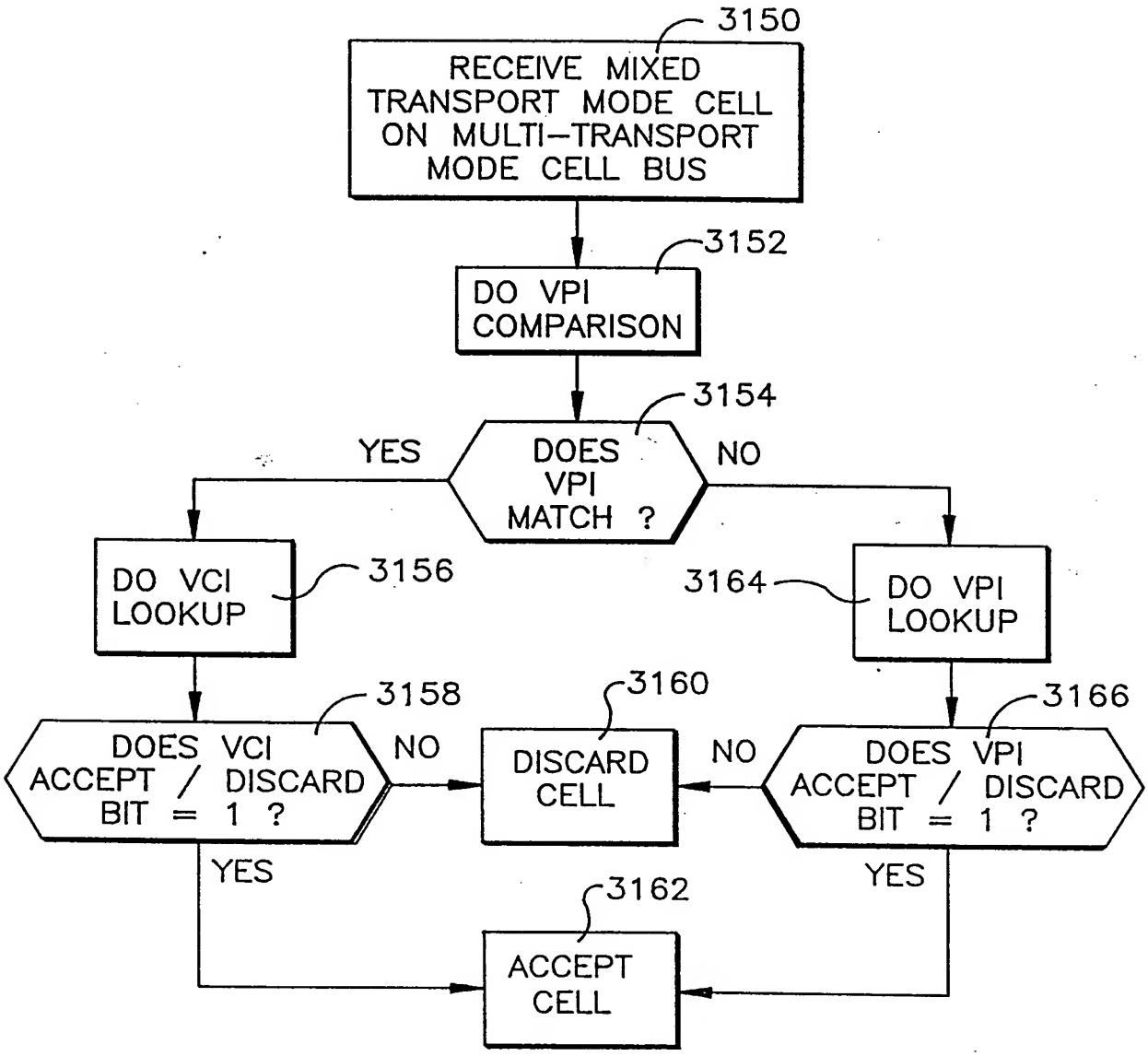

3100
RECEIVE MIXED TRAFFIC CELL ON MULTI-TRANSPORT MODE CELL BUS
3102
DO VPI COMPARISON
3104
DOES VPI MATCH ?
NO
3106
DISCARD CELL
YES
3108
DO VCI LOOKUP USING VCI LOOKUP TABLE
3110
DOES VCI ACCEPT/ DISCARD BIT = 1 ?
NO
YES
3112
AAL1 OR AAL5 ?
NO
AAL5
3114
FORWARD CELL TO AAL5 SAR
AAL1
YES
3116
LOWER VCI TRANSLATION
3118
FORWARD TO AAL1 SAR

Fig. 31A

Fig. 31B


3150
RECEIVE MIXED TRANSPORT MODE CELL ON MULTI-TRANSPORT MODE CELL BUS
3152
DO VPI COMPARISON
3154
DOES VPI MATCH ?
YES
NO
DO VCI LOOKUP
3156
3164
DO VPI LOOKUP
3158
DOES VCI ACCEPT / DISCARD BIT = 1 ?
NO
3160
DISCARD CELL
NO
3166
DOES VPI ACCEPT / DISCARD BIT = 1 ?
YES
YES
3162
ACCEPT CELL

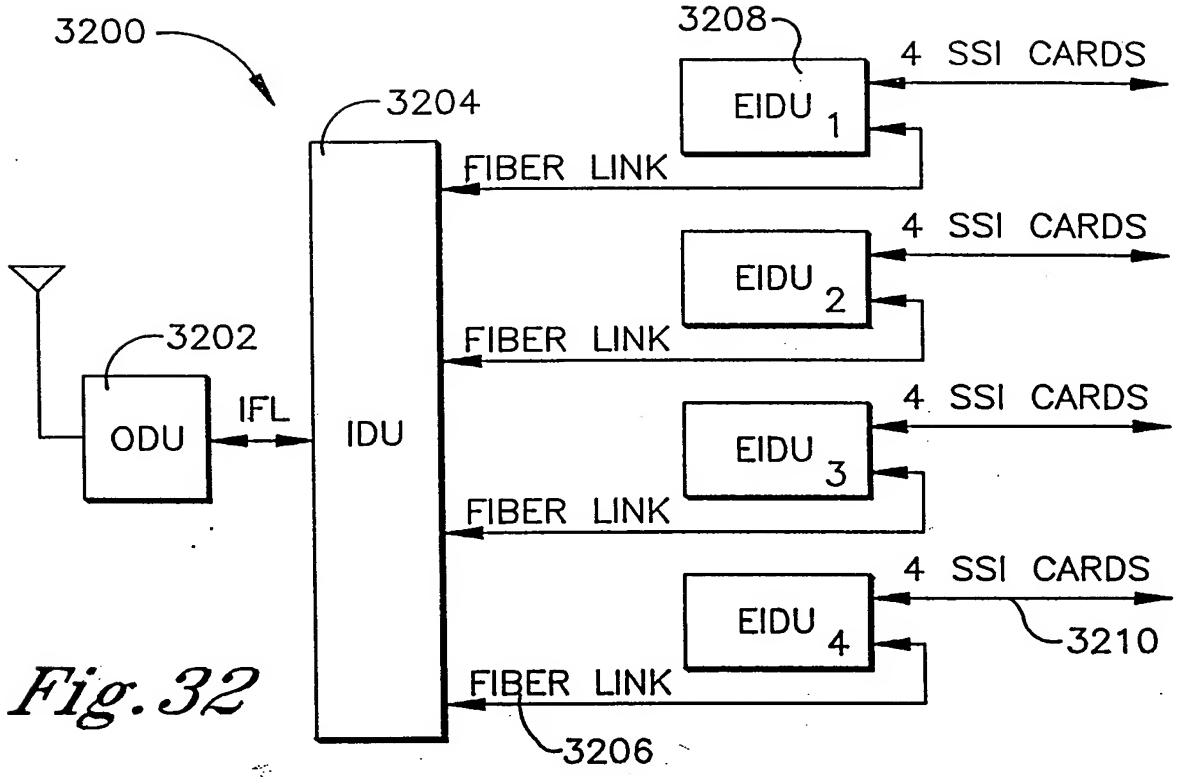

3200
3208
4 SSI CARDS
EIDU 1
3204
FIBER LINK
4 SSI CARDS
EIDU 2
3202
FIBER LINK
ODU
IFL
IDU
4 SSI CARDS
EIDU 3
FIBER LINK
4 SSI CARDS
EIDU 4
3210
FIBER LINK
3206

Fig. 32

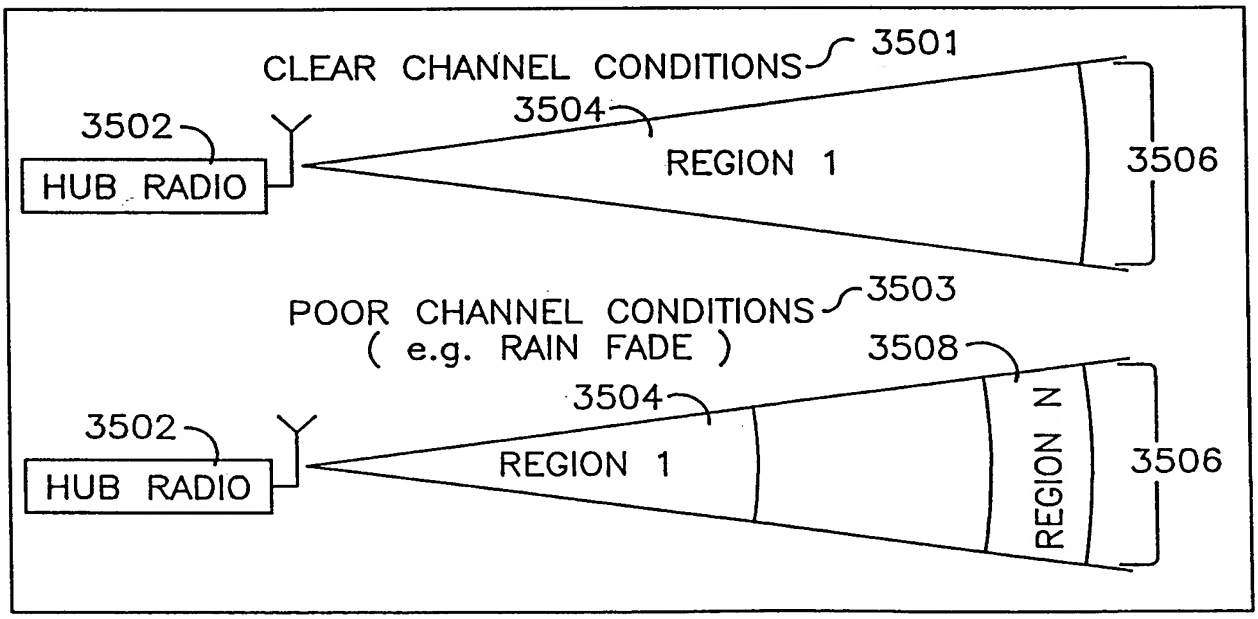

CLEAR CHANNEL CONDITIONS
3501
3502
3504
HUB RADIO
REGION 1
3506
POOR CHANNEL CONDITIONS
(e.g. RAIN FADE)
3503
3508
3504
3502
REGION 1
REGION N
HUB RADIO
3506

Fig. 35

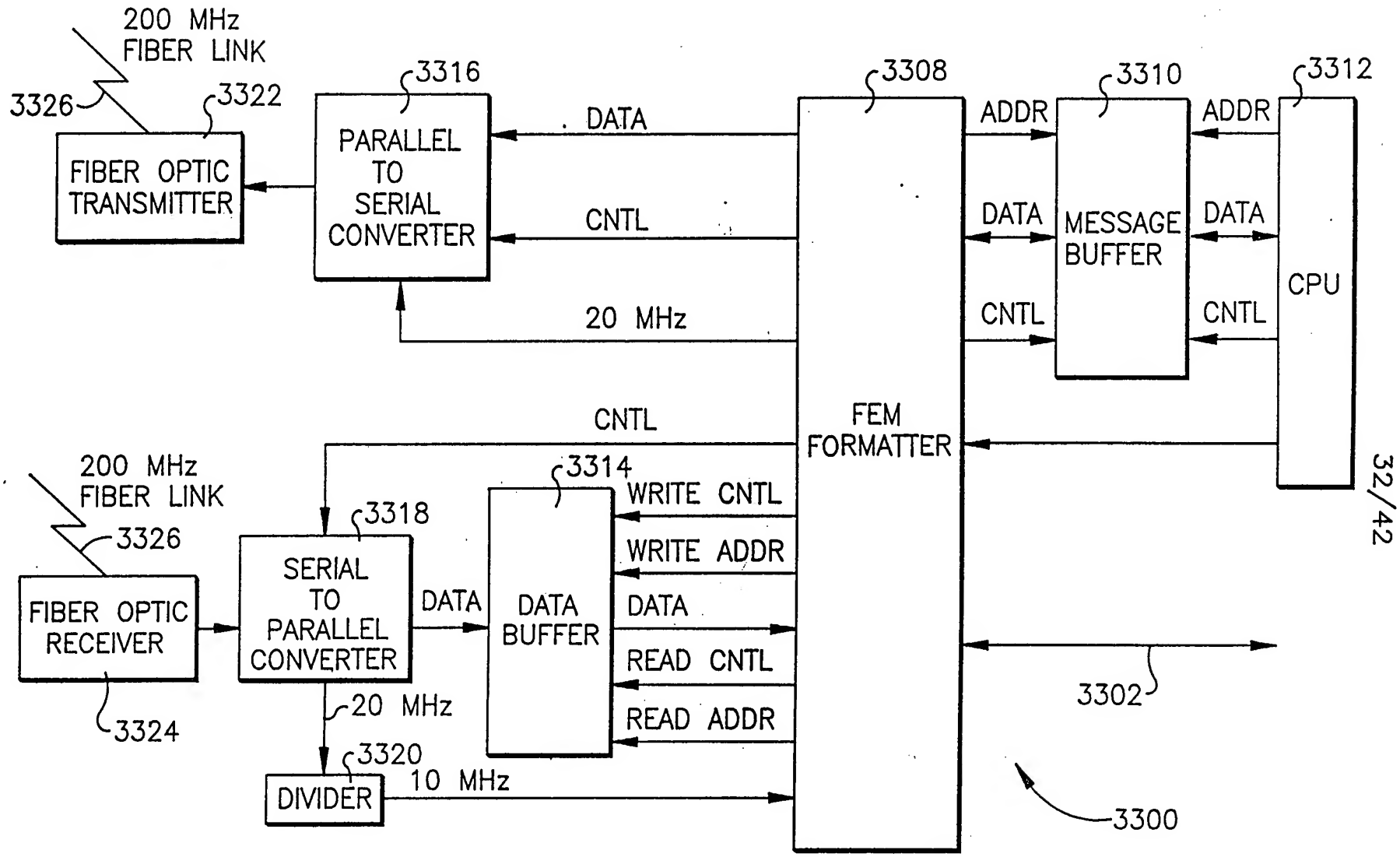

200 MHz
FIBER LINK
3326
3322
FIBER OPTIC
TRANSMITTER
3316
PARALLEL
TO
SERIAL
CONVERTER
DATA
CNTL
20 MHz
3308
FEM
FORMATTER
3310
MESSAGE
BUFFER
3312
CPU
ADDR
ADDR
DATA
DATA
CNTL
CNTL
CNTL
200 MHz
FIBER LINK
3326
FIBER OPTIC
RECEIVER
3324
3318
SERIAL
TO
PARALLEL
CONVERTER
DATA
20 MHz
3320
DIVIDER
10 MHz
3314
DATA
BUFFER
WRITE CNTL
WRITE ADDR
DATA
READ CNTL
READ ADDR
3302
3300
32/42

Fig. 33

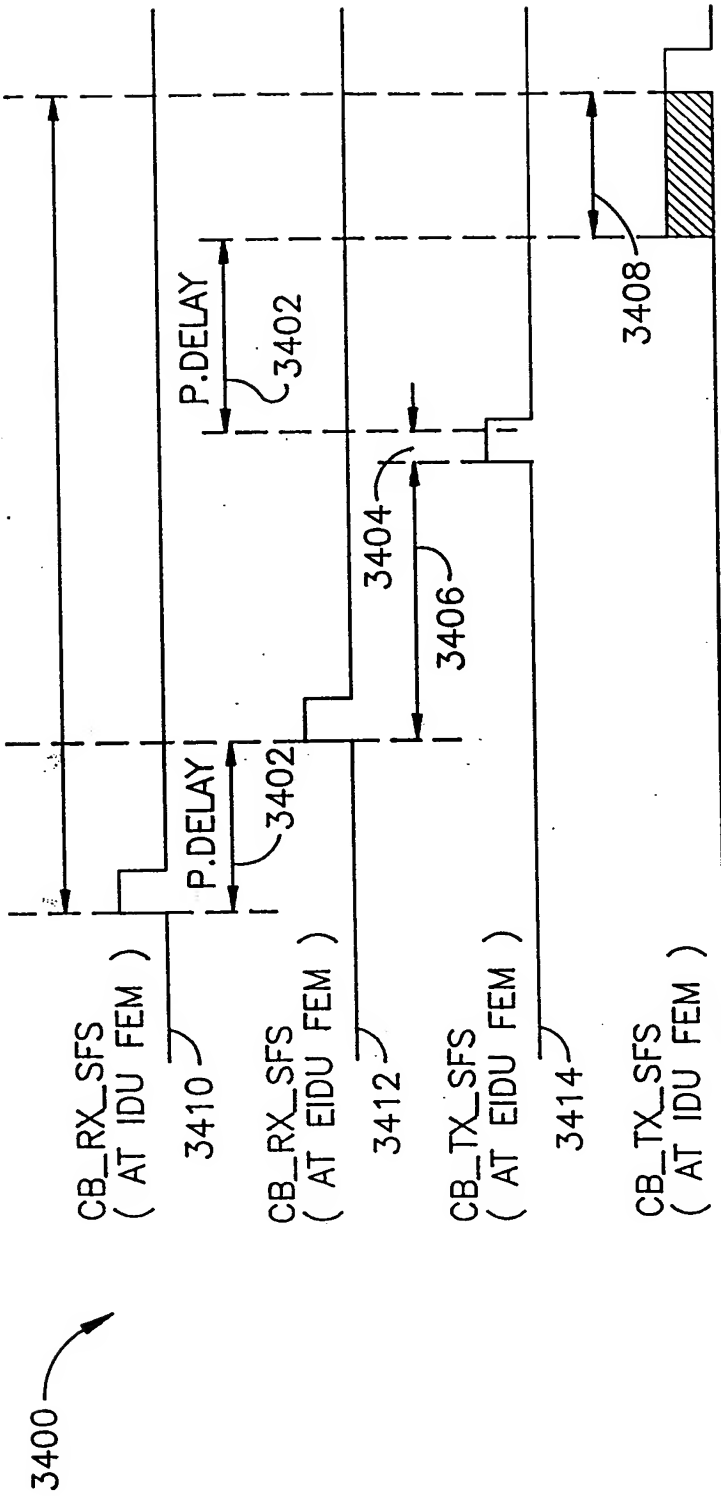

3400
CB_RX_SFS
(AT IDU FEM)
3410
P.DELAY
3402
CB_RX_SFS
(AT EIDU FEM)
3412
3404
3406
CB_TX_SFS
(AT EIDU FEM)
3414
3408
CB_TX_SFS
(AT IDU FEM)
3416

Fig. 34

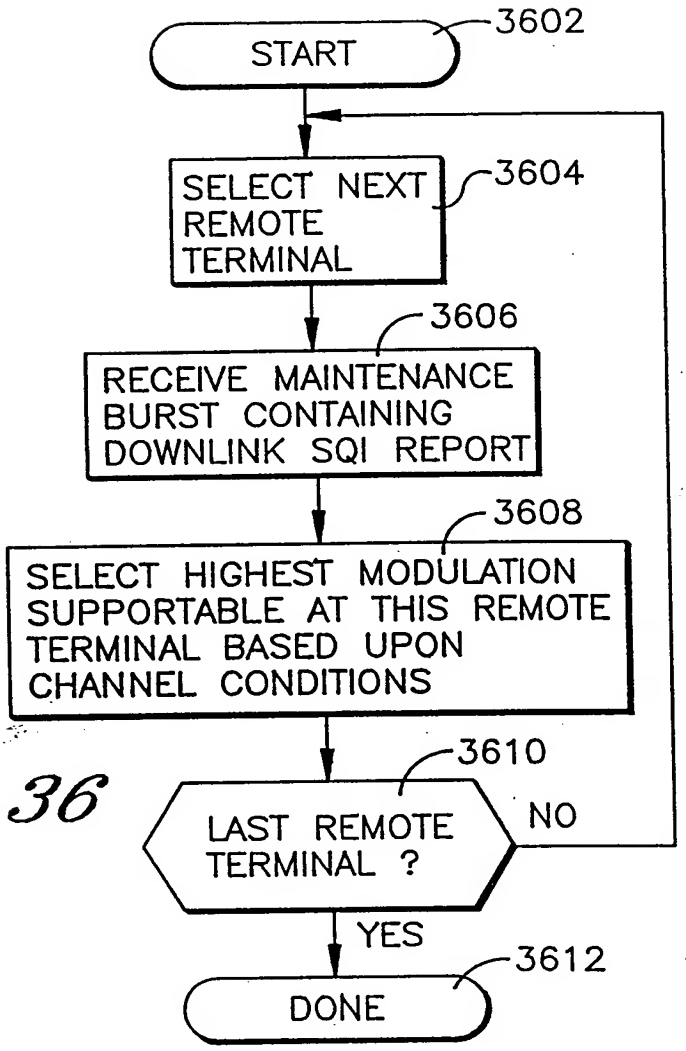

START
3602
SELECT NEXT REMOTE TERMINAL
3604
RECEIVE MAINTENANCE BURST CONTAINING DOWNLINK SQI REPORT
3606
SELECT HIGHEST MODULATION SUPPORTABLE AT THIS REMOTE TERMINAL BASED UPON CHANNEL CONDITIONS
3608
LAST REMOTE TERMINAL ?
3610
NO
YES
DONE
3612

Fig. 36

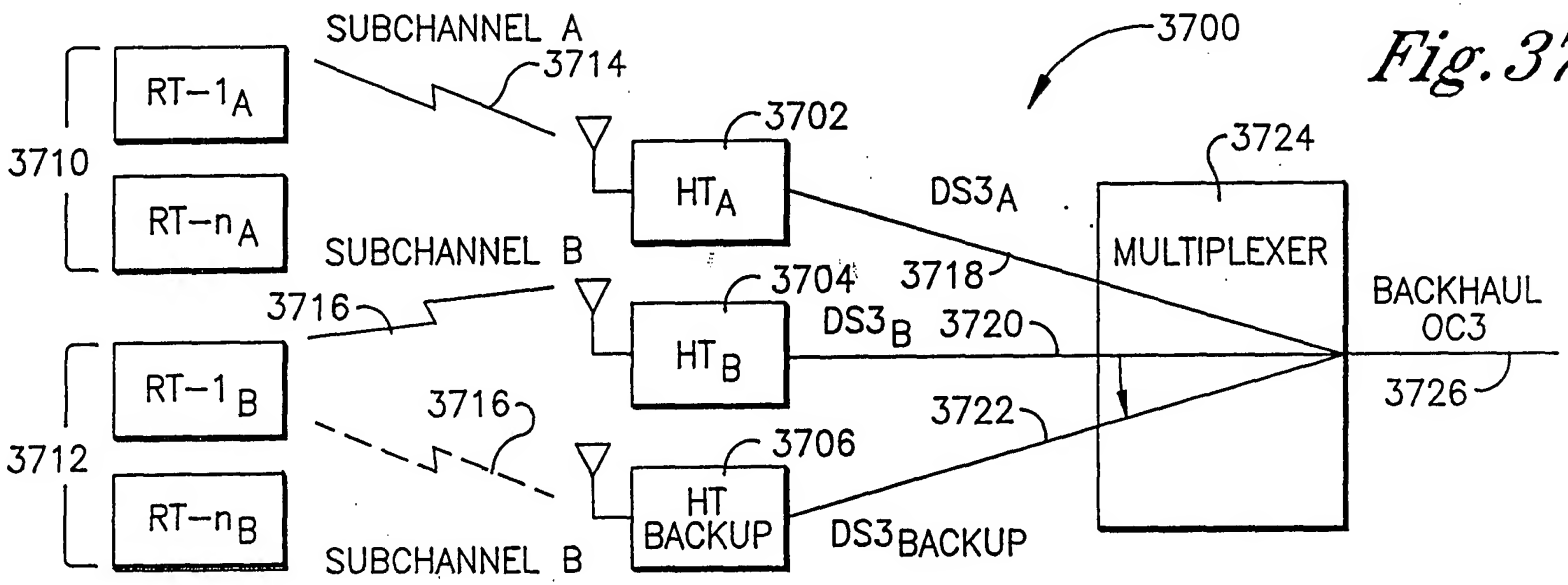

SUBCHANNEL A
3714
3700
3702
3724
RT–1A
RT–nA
3710
HTA
DS3A
MULTIPLEXER
SUBCHANNEL B
3704
3718
3716
HTB
DS3B
3720
BACKHAUL
OC3
3726
RT–1B
3716
3722
3706
3712
RT–nB
HT
BACKUP
DS3BACKUP
SUBCHANNEL B

Fig. 37

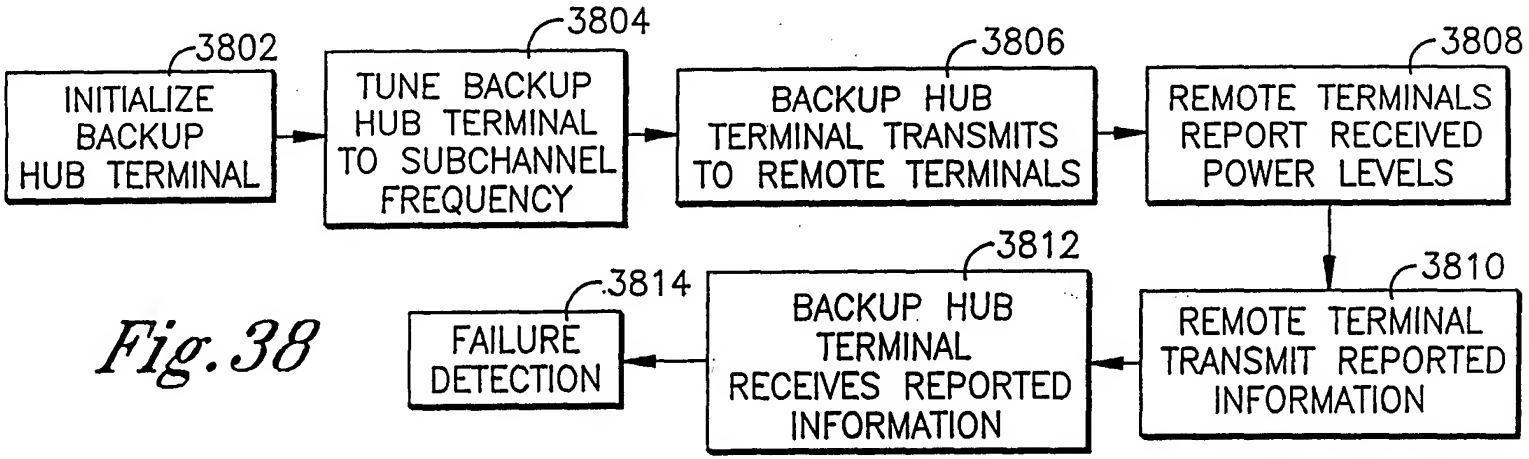
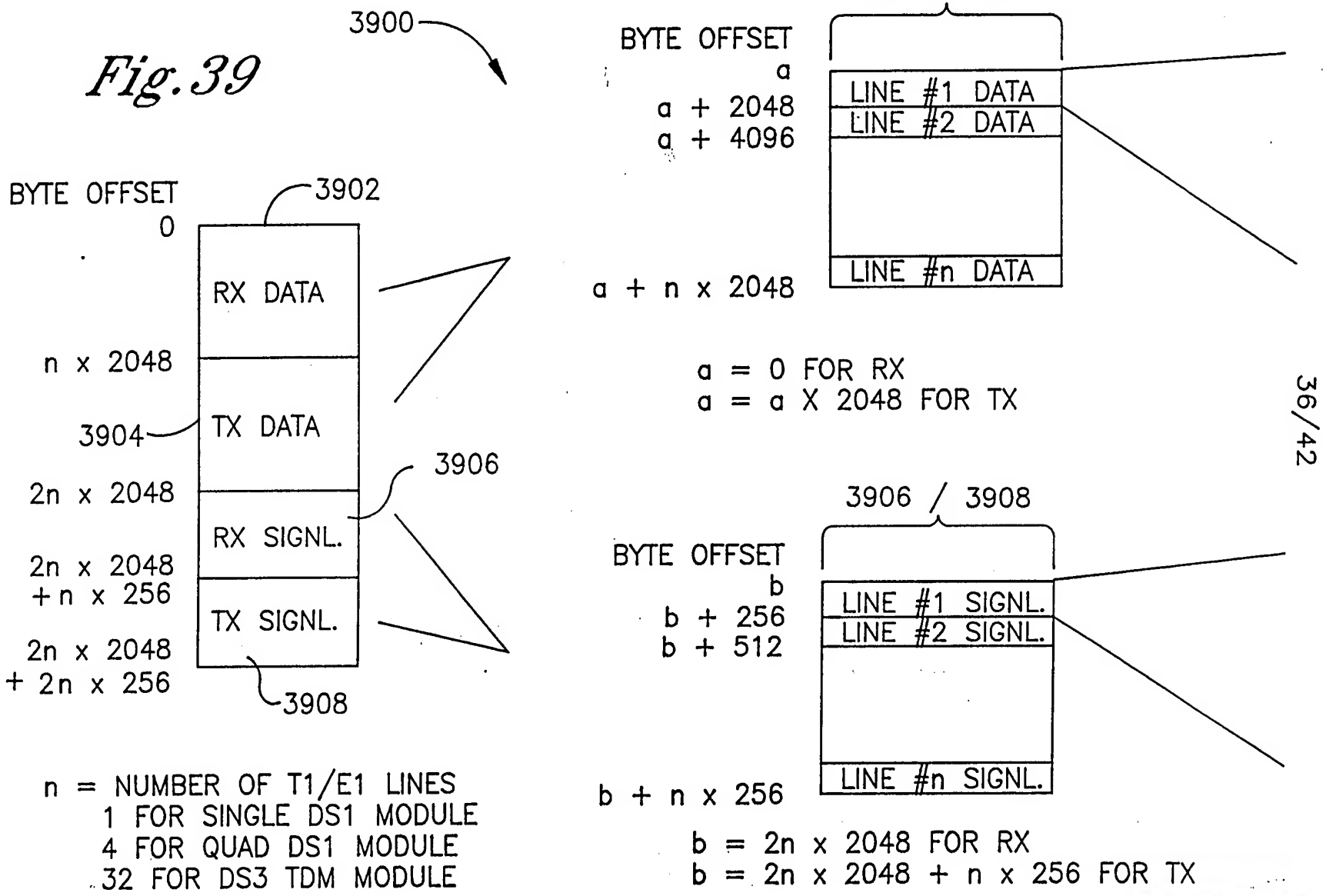

3802
INITIALIZE BACKUP HUB TERMINAL
3804
TUNE BACKUP HUB TERMINAL TO SUBCHANNEL FREQUENCY
3806
BACKUP HUB TERMINAL TRANSMITS TO REMOTE TERMINALS
3808
REMOTE TERMINALS REPORT RECEIVED POWER LEVELS
3810
REMOTE TERMINAL TRANSMIT REPORTED INFORMATION
3812
BACKUP HUB TERMINAL RECEIVES REPORTED INFORMATION
3814
FAILURE DETECTION

Fig. 38

Fig. 39


3900
BYTE OFFSET
0
3902
RX DATA
n x 2048
TX DATA
3904
2n x 2048
3906
RX SIGNL.
2n x 2048
+n x 256
TX SIGNL.
2n x 2048
+ 2n x 256
3908
n = NUMBER OF T1/E1 LINES
1 FOR SINGLE DS1 MODULE
4 FOR QUAD DS1 MODULE
32 FOR DS3 TDM MODULE
3902 / 3904
BYTE OFFSET
a
a + 2048
a + 4096
LINE #1 DATA
LINE #2 DATA
LINE #n DATA
a + n x 2048
a = 0 FOR RX
a = a X 2048 FOR TX
3906 / 3908
BYTE OFFSET
b
b + 256
b + 512
LINE #1 SIGNL.
LINE #2 SIGNL.
LINE #n SIGNL.
b + n x 256
b = 2n x 2048 FOR RX
b = 2n x 2048 + n x 256 FOR TX

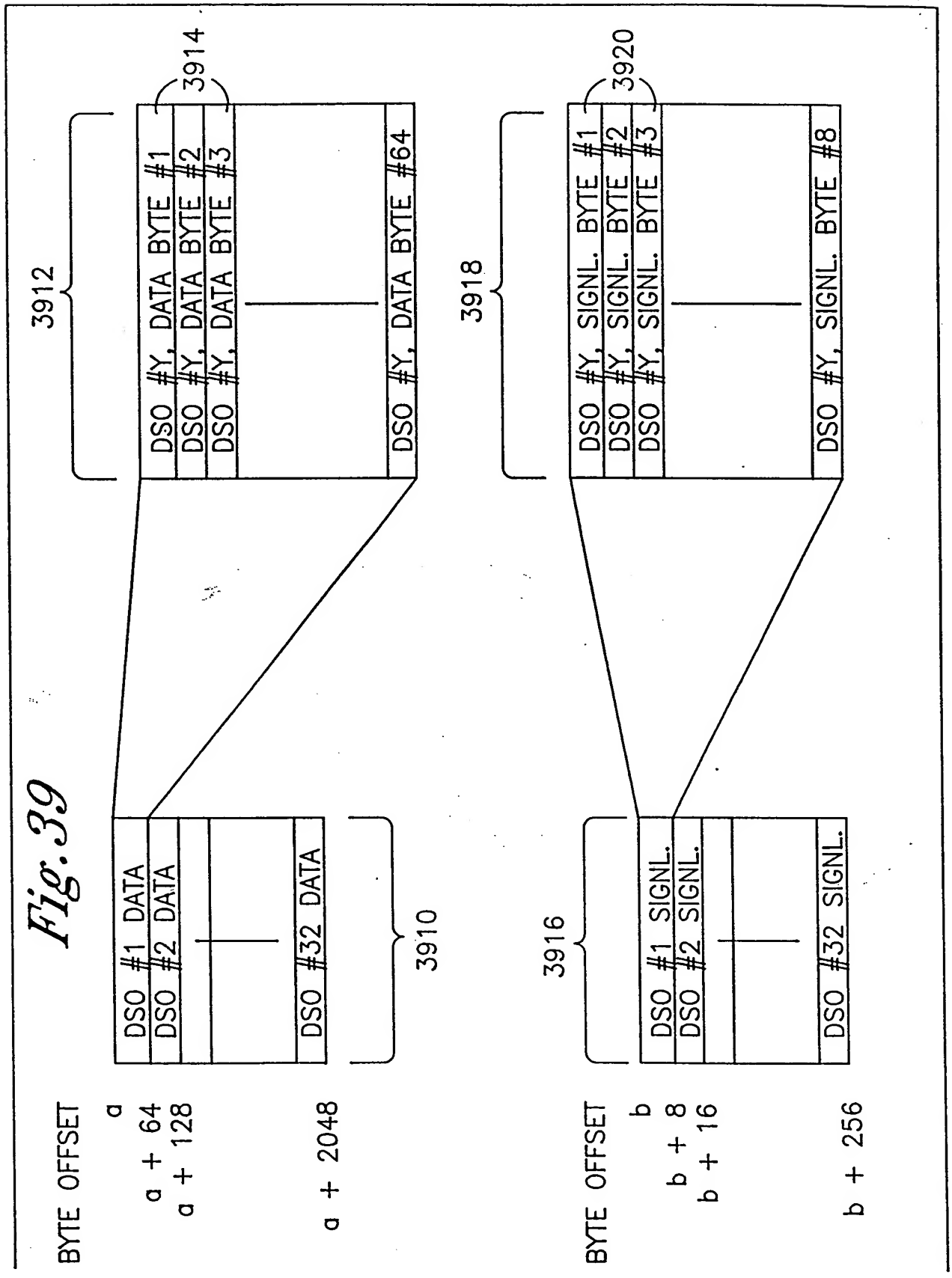

BYTE OFFSET
a
a + 64
a + 128
a + 2048
DSO #1 DATA
DSO #2 DATA
DSO #32 DATA
3910
3912
DSO #Y, DATA BYTE #1
DSO #Y, DATA BYTE #2
DSO #Y, DATA BYTE #3
DSO #Y, DATA BYTE #64
3914
BYTE OFFSET
b
b + 8
b + 16
b + 256
DSO #1 SIGNL.
DSO #2 SIGNL.
DSO #32 SIGNL.
3916
3918
DSO #Y, SIGNL. BYTE #1
DSO #Y, SIGNL. BYTE #2
DSO #Y, SIGNL. BYTE #3
DSO #Y, SIGNL. BYTE #8
3920

Fig. 39

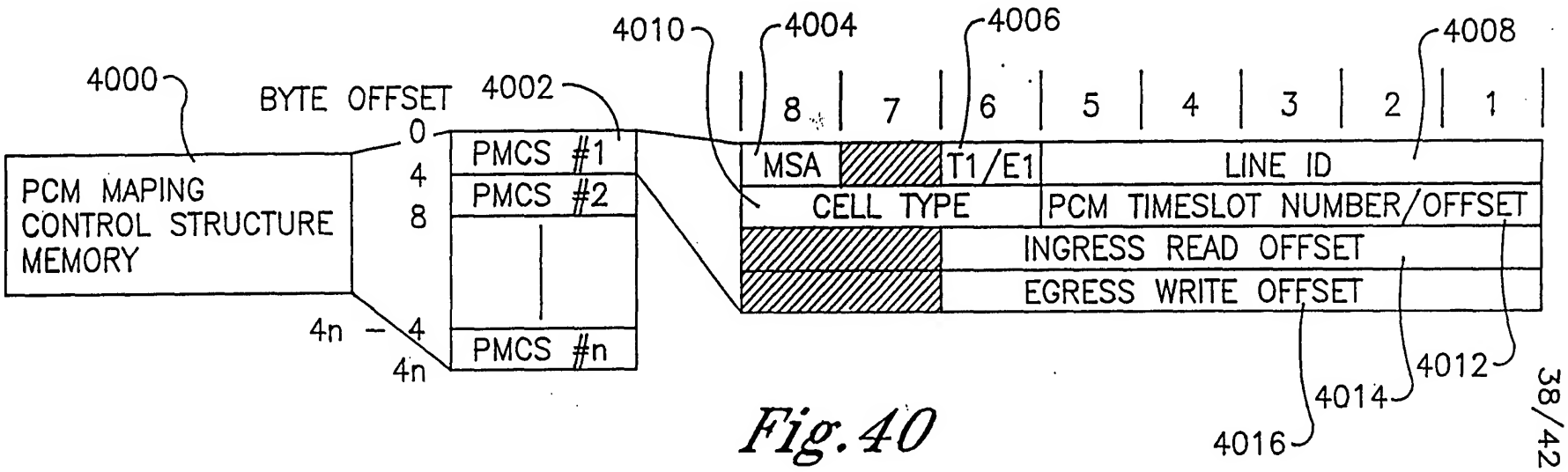

4000
PCM MAPING CONTROL STRUCTURE MEMORY
BYTE OFFSET
4002
0
4
8
4n – 4
4n
PMCS #1
PMCS #2
PMCS #n
4010
4004
4006
4008
8
7
6
5
4
3
2
1
MSA
T1/E1
LINE ID
CELL TYPE
PCM TIMESLOT NUMBER/OFFSET
INGRESS READ OFFSET
EGRESS WRITE OFFSET
4012
4014
4016

Fig. 40

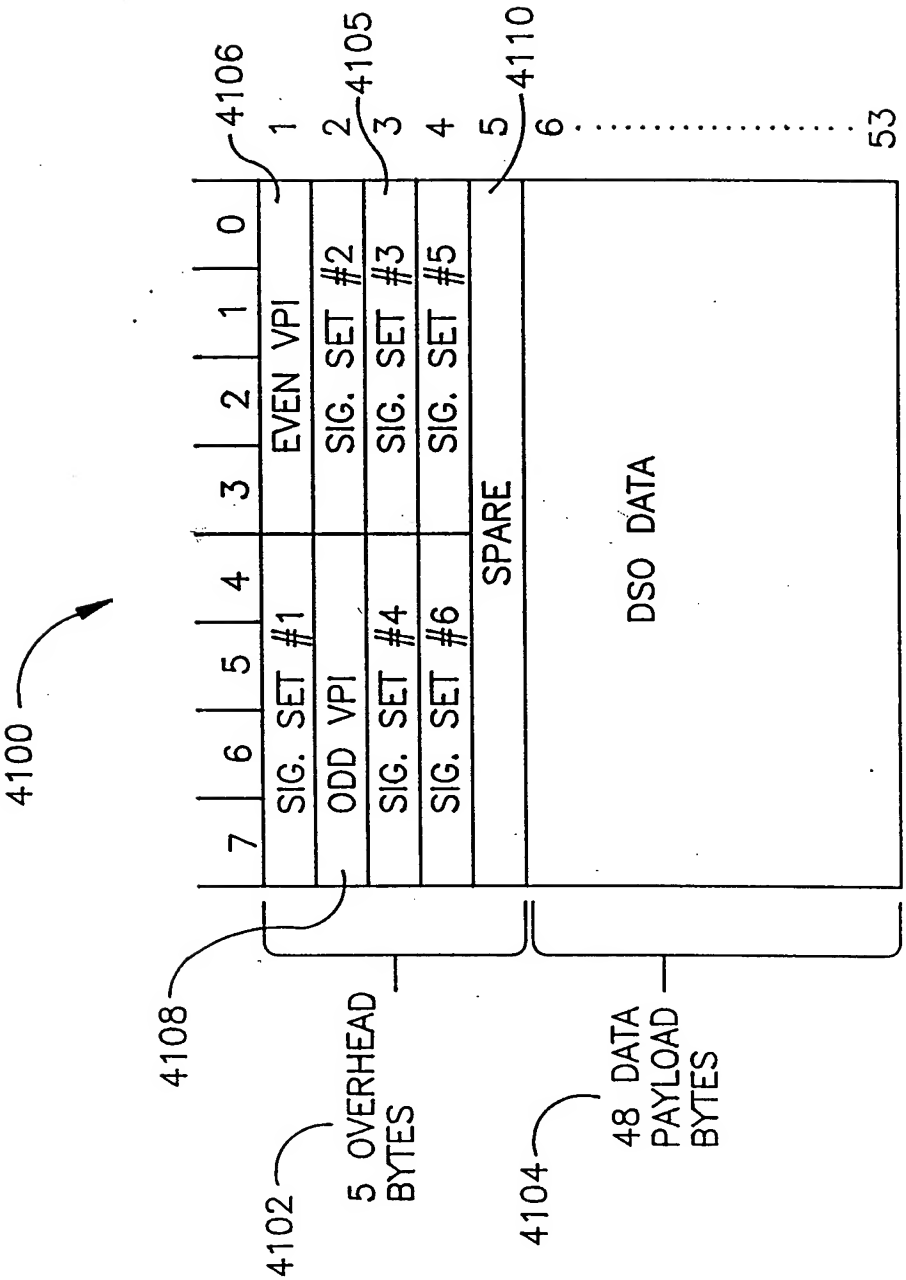

4100
7
6
5
4
3
2
1
0
SIG. SET #1
ODD VPI
SIG. SET #4
SIG. SET #6
EVEN VPI
SIG. SET #2
SIG. SET #3
SIG. SET #5
SPARE
DSO DATA
4106
4105
4110
1
2
3
4
5
6
53
4108
4102
5 OVERHEAD BYTES
4104
48 DATA PAYLOAD BYTES

Fig. 41

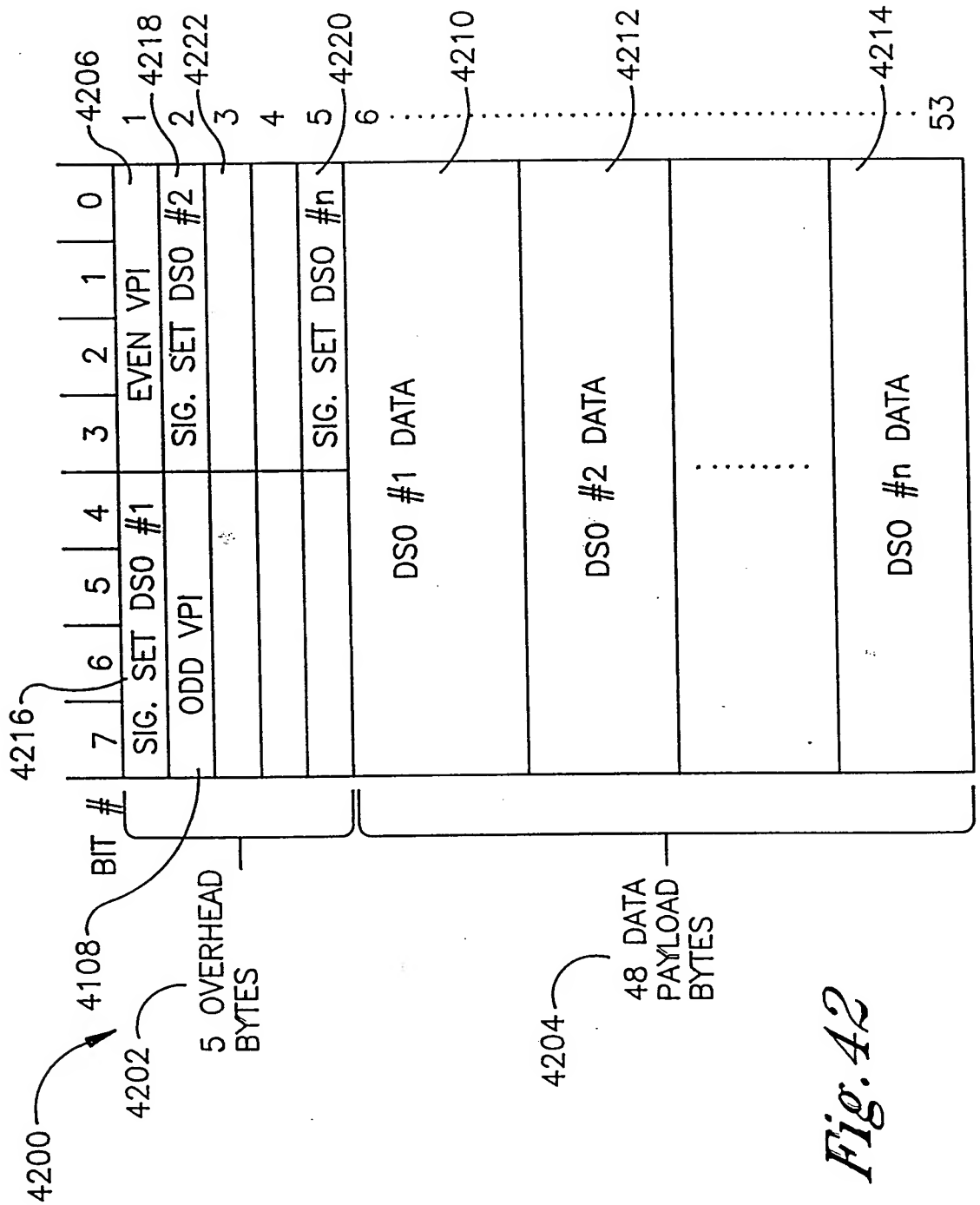

4200
4202
4108
4216
BIT #
7
6
5
4
3
2
1
0
SIG. SET DSO #1
ODD VPI
EVEN VPI
SIG. SET DSO #2
SIG. SET DSO #n
4206
1
4218
2
4222
3
4
5
4220
6
4210
4212
4214
53
DSO #1 DATA
DSO #2 DATA
DSO #n DATA
5 OVERHEAD BYTES
4204
48 DATA PAYLOAD BYTES

Fig. 42

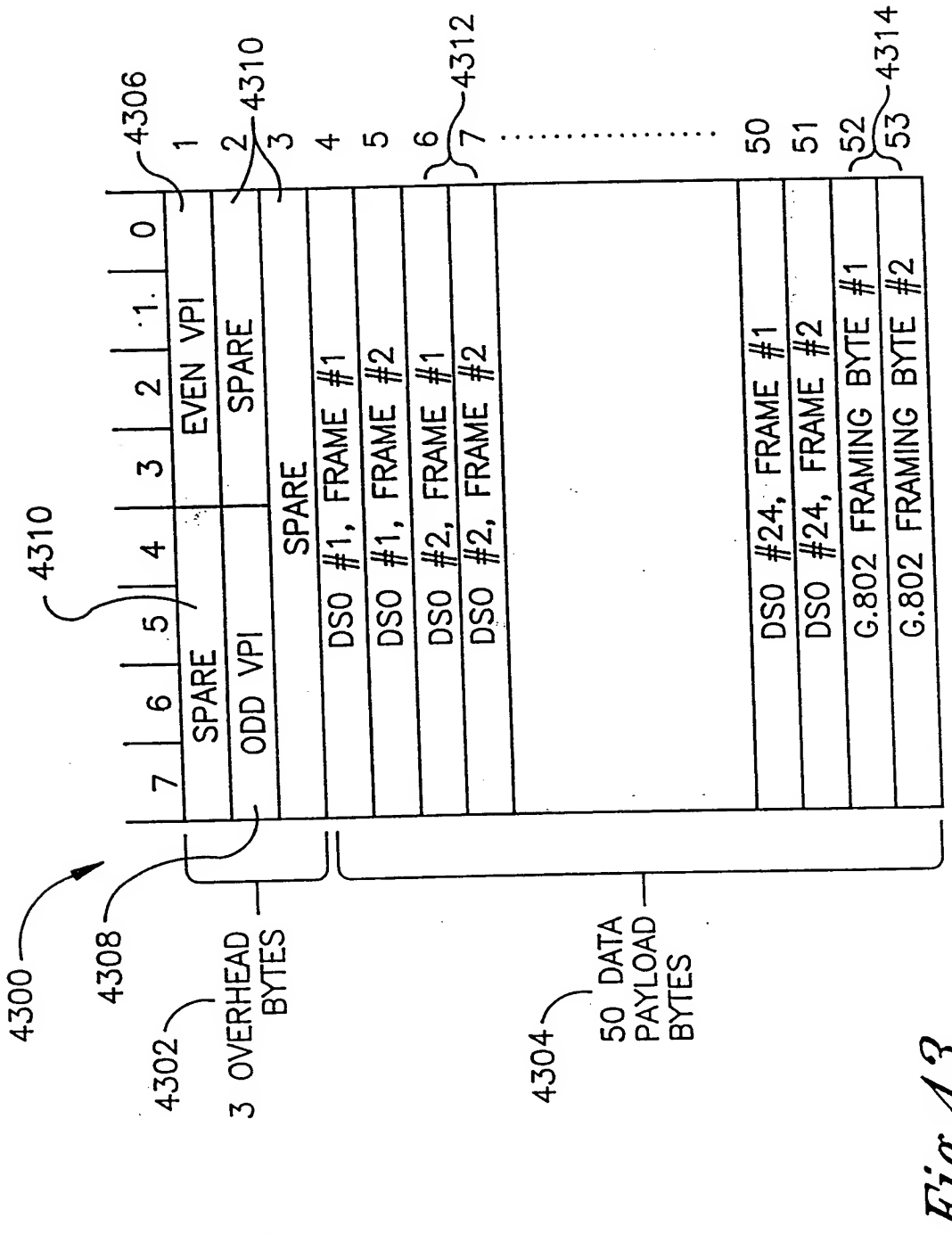

4300
4308
4302
3 OVERHEAD BYTES
4304
50 DATA PAYLOAD BYTES
4310
4306
4310
4312
4314
7 6 5 4 3 2 1 0
1 2 3 4 5 6 7 ..... 50 51 52 53
SPARE
ODD VPI
SPARE
EVEN VPI
SPARE
DS0 #1, FRAME #1
DS0 #1, FRAME #2
DS0 #2, FRAME #1
DS0 #2, FRAME #2
DS0 #24, FRAME #1
DS0 #24, FRAME #2
G.802 FRAMING BYTE #1
G.802 FRAMING BYTE #2

Fig. 43

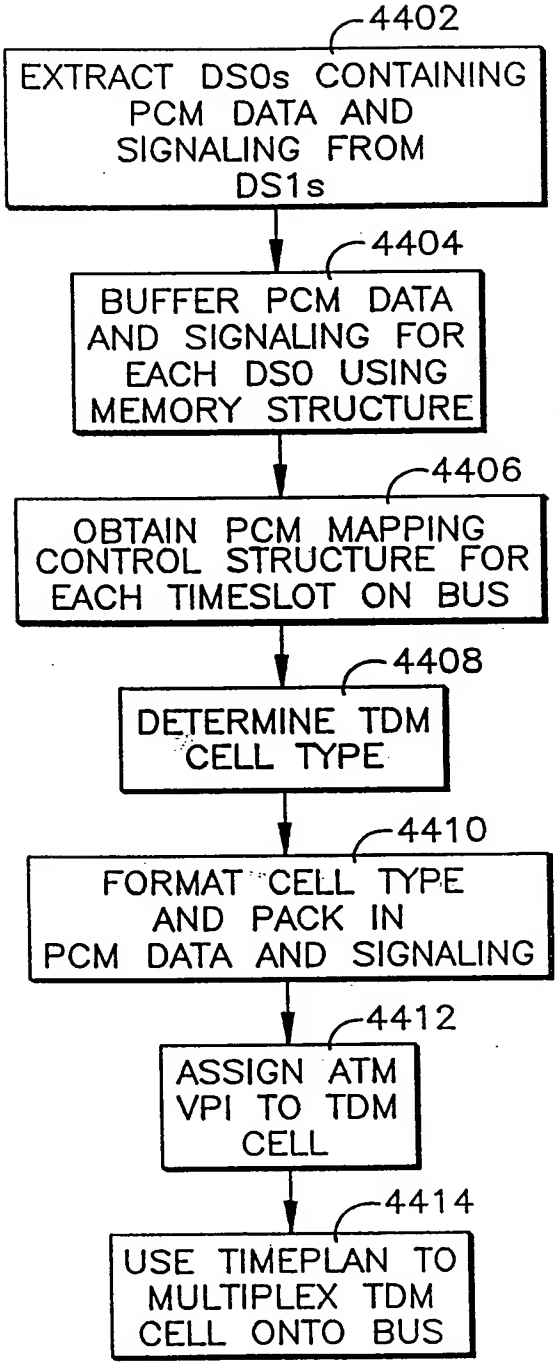


Fig. 44A

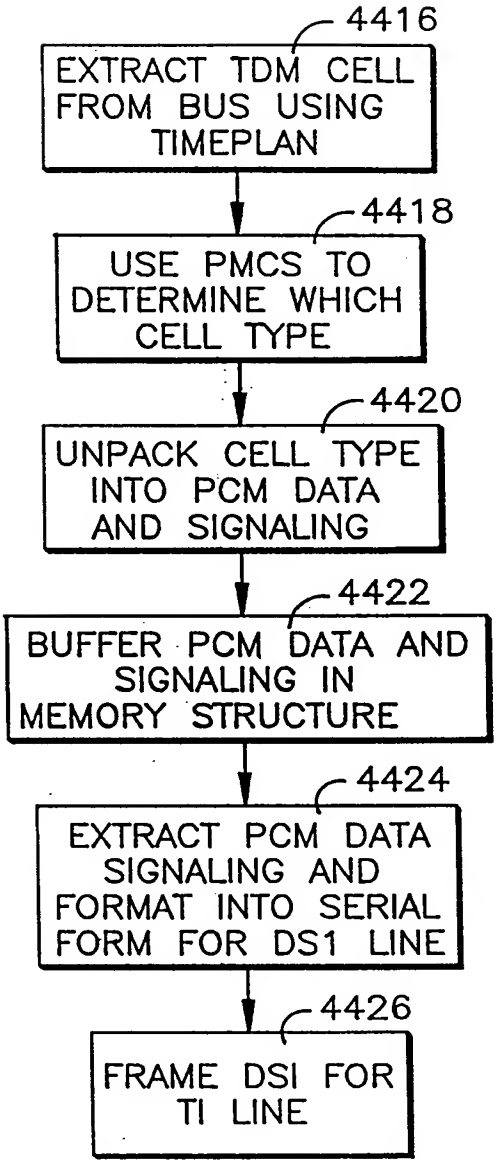


Fig. 44B